CONCORD INSTRUMENT
DIVISION

MODEL 1253H

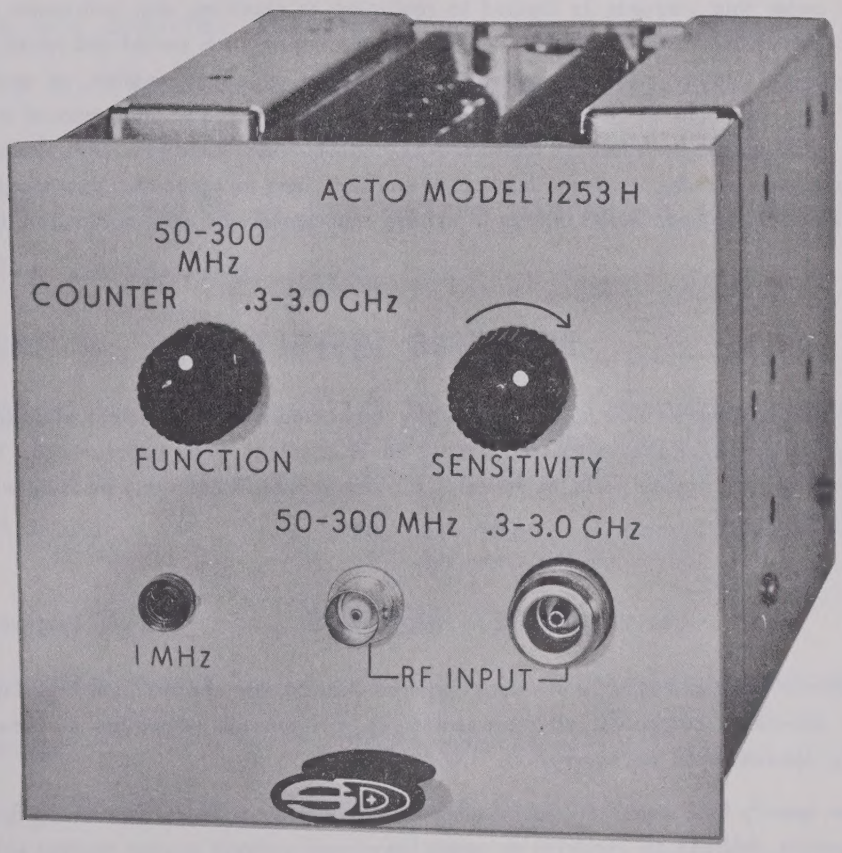
ACTO PRESCALER
PLUG-IN

SYSTRON DONNER

D-N-181 TEST

Concord Instrument Division

INSTRUCTION MANUAL



CONCORD INSTRUMENT DIVISION

MODEL 1253H

ACTO PRESCALER PLUG-IN

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SYSTRON DONNER CORPORATION

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SYSTRON DONNER
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WARRANTY

Systron-Donner instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. This warranty does not apply to vacuum tubes, except as they are warranted by tube manufacturers. The liability of Seller under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer at his expense during such period and which has not been subjected to misuse, neglect, improper installations, repair, alteration, or accident. Seller shall have the right of final determination as to the existence and cause of a defect. In no event shall Seller be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, express, implied or statutory, and no agreement extending or modifying it will be binding upon Seller unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Systron Donner instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the unit is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company.

REPAIRS

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative or Sales Manager, Instruments, Systron-Donner Corporation, 888 Galindo Street, Concord, California.

ADDENDA

1253H PRESCALER/ACTO® PLUG-IN

A. GENERAL DESCRIPTION

The Model 1253H is a combination Prescaler/ACTO® and produces instantaneous, direct readout of CW input frequencies. Since the measuring technique is completely automatic, the operator is not required to make any calculations or control settings. Measurements are counter accurate, and the final answer appears automatically in two seconds or less, depending upon the frequency being measured and the resolution desired. The 1253H is ideal for instant measurements of noise-free microwave signals and automatic tracking of varying inputs.

B. SPECIFICATIONS

Frequency Range	DC to 50 MHz (through Counter's "C" input), 50 MHz to 300 MHz (Prescaler input), 300 MHz to 3 GHz (ACTO® input).
Input Sensitivity	Better than -7 dbm (100 mV rms (typically -12 to -15 dbm)
Maximum Useable Input	+7 dbm (500 mV rms)
Maximum Allowable Input	+20 dbm (2.2 V rms); ±125 VDC
Input Impedance	50Ω (nominal)
Accuracy	Same as Counter
FM Tolerance	Maximum of 0.1% FM (f_M = 60 Hz0 decreasing by a factor of 0.5% per octave of fm above 60 Hz.
Maximum Amplitued Modulation (400 Hz to 1 kHz)	70%
Lock-On Range	Approx. 2% of input frequency

Sweep Rate (within any Lock-On Range)	12% f_i/sec; f_i = instantaneous input frequency.
Resolution	0.1 Hz to 100 kHz in decade steps selected by counter time base switch.
Registration	Automatic, direct registration with positioned decimal.

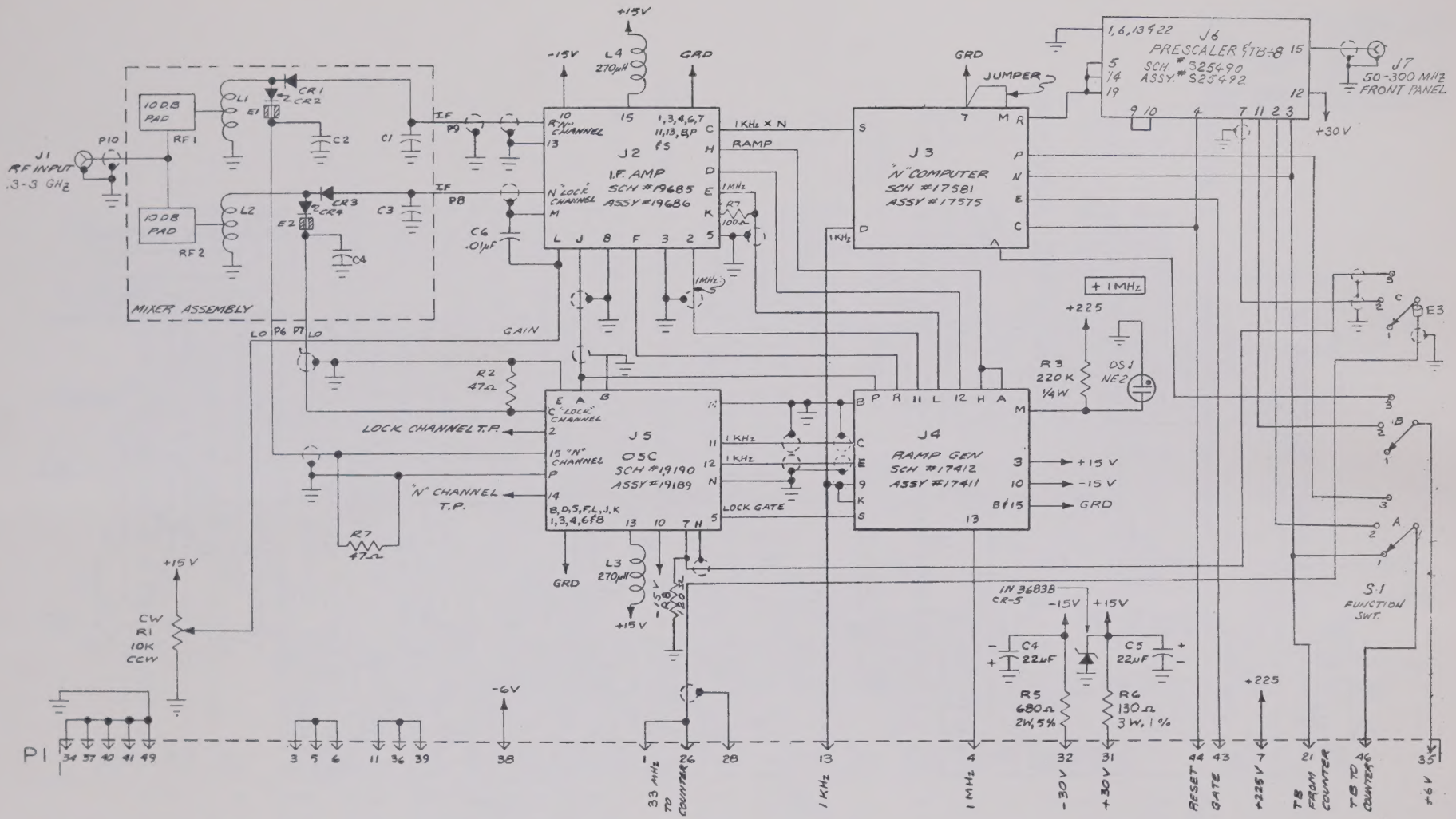
C. OPERATION (Refer to Schematic Block Diagram dwg. S25592)

Three modes of operation are available with the 1253H: 1) Counter; 2) Prescaler (50-300 MHz); and 3) ACTO (0.3-3.0 GHz). Selection is made by the front panel FUNCTION switch and connection of the signal to be measured to the appropriate input connector.

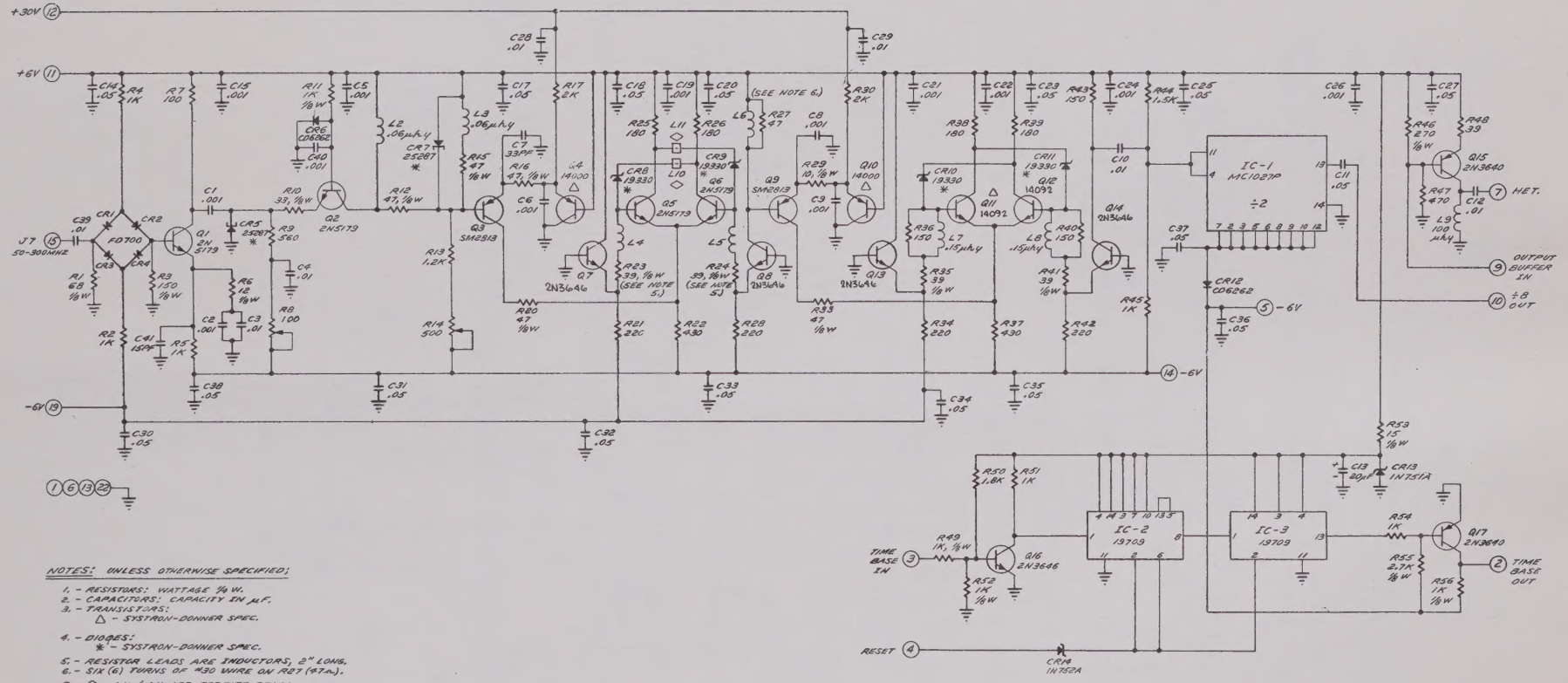
In the COUNTER mode, normal counter operation is provided for signals in the 0-50 MHz range. When the Prescaler mode is selected, the signal in the range of 50-300 MHz is applied to J7 (RF INPUT 50-300 MHz) on the 1253H front panel and a direct readout is obtained on the counter. In the ACTO mode, signals in the 0.3 to 3 GHz range are applied to J1 (with 1 MHz offset) is obtained on the counter.

D. PRESCALER BOARD LOCATION

The Prescaler Assembly is mounted on the rear of the plug-in under a protective cover.



SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	SCHEMATIC BLOCK DIAGRAM MODEL 1253H ACTO	
MATERIAL	DWG NO. 525592	ISSUE B



NOTES: UNLESS OTHERWISE SPECIFIED;

1. - RESISTORS: WATTAGE 1/8 W.
2. - CAPACITORS: CAPACITY IN μF.
3. - TRANSISTORS:
   △ - SYSTRON-DONNER SPEC.
4. - DIODES:
   * - SYSTRON-DONNER SPEC.
5. - RESISTOR LEADS ARE INDUCTORS, 2" LONG.
6. - SIX (6) TURNS OF #30 WIRE ON R27 (47Ω).
7. - ◇ - L10 & L11 ARE FERRITE BEADS.

SYSTRON DONNER CORPORATION, CONCORD, CALIFORNIA	SCHEMATIC, PRESCALER & T.B. ÷8 BD.
MATERIAL	DWG NO. S 25490 — ISSUE E

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CHAPTER 1 — GENERAL INFORMATION

1-1. FUNCTIONS

The ACTO* series plug-in units are capable of measuring continuous wave frequencies in the range of 300 megahertz to 12.4 gigahertz. They are used in conjunction with Systron-Donner's 50 and 100 megahertz frequency counters.

The 300 megahertz to 12.4 gigahertz range is covered by three separate plug-in units. The Model 1253 which has a range of 300 megahertz to 3.0 gigahertz, the Model 1254 which has a range of 2.96 gigahertz to 8.2 gigahertz, and the Model 1255 with a range of 8.2 gigahertz to 12.4 gigahertz.

1-2. STANDARD FEATURES

The ACTO series features completely automatic measurement of microwave frequencies. Measurements may be made by unskilled persons with ease and accuracy. Accuracy of measurement is completely independent of operator skill.

The accuracy of measurements made with the ACTO series is the same as of the counter it is used with. (±1 count, ± time base stability) Measurement resolution is ±0.1 hz to ±100K hz selectable in decade steps by the counter time base switch.

1-3. OPTIONAL FEATURES

There are three principle options for the ACTO series plug-ins.

1) Options to either increase or decrease sensitivity are available. They are available individually on a factory option basis.

2) Range Extension Option: The frequency range of any of the ACTO models may be extended on a factory option basis.

3) W Option: The W option adds circuitry which makes the ACTO models compatible with the Hewlett-Packard Model 5245L and Model 5246L counters. No modification of the Hewlett-Packard counters is required.

1-4. TECHNIQUE

The ACTO series uses the transfer oscillator technique combined with a unique harmonic number computer. (ACTO is an acroynm for Automatic Computing Transfer Oscillator.)

In the ACTO an internal swept oscillator is phase-locked to the input frequency with a precise minus 1 M hz offset.

The oscillator output is then divided by two and applied to the counter input. Simultaneously the swept oscillator frequency is shifted by 1K hz and applied to a second mixer. The input frequency is also applied to the mixer resulting in an output equal to 1 M hz (the offset) plus 1K hz times the harmonic number (n). This output is applied to an IF amplifier and then to another mixer where the 1 M hz is removed. The N (harmonic number) is then computed and the counter time base multiplied times N. The result is a counter display equal to the input frequency minus 1 M hz.

SPECIFICATIONS

Frequency range:
Model 1253: 300 MHz to 3000 MHz
Model 1254: 2.96 GHz to 8.2 GHz
Model 1255: 8.2 GHz to 12.4 GHz

Type of input signals: CW, with or without AM.

Signal input sensitivity: Better than —7 dbm (100 mv rms), typically —10 to —20 dbm.

Lock-on time: .4 sec. after time base pulse (max.), .2 sec. typical.

Maximum useable signal level: +7 dbm.

Maximum level without damage: 100 mw (2.23 v.).

Impedance: 50Ω nominal.

Connector: Type N.

Accuracy: Retains accuracy of basic counter (±1 count, ±time base stability).

Resolution: ±0.1 Hz to ±100 kHz selectable in decade steps by counter time base switch.

Controls

Sensitivity: For attenuation of high signal levels.

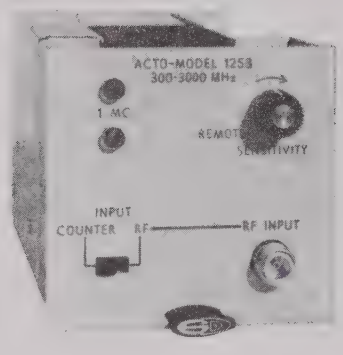
Input selector: "COUNTER—RF" switch for using counter without disconnecting plug-in.

Readout: Digital presentation of microwave frequency by basic counter. Readout is in-line with units annunciator and automatic decimal point. 1 MHz offset indicated by "+" indicator light on plug-in.8 digits standard on Models 1037 and 1038; 7 digits and 6 digits standard on Models 1018 and 1017 respectively, up to 8 digits with Option E.

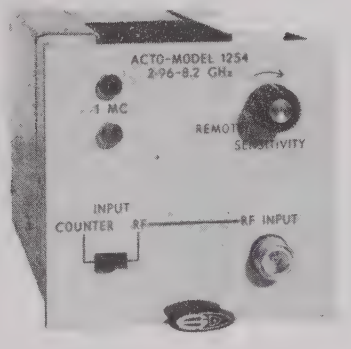
Power: From basic counter (10 watts).

Environmental conditions: —20°C to +65°C.

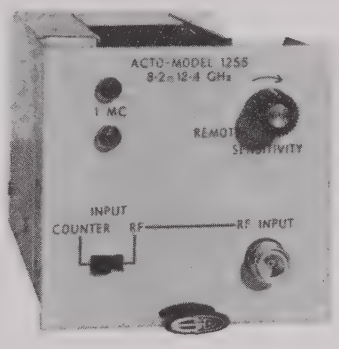
Automatic ACTO® Plug-ins



Model 1253
300 - 3000 MHz



Model 1254
2.96 - 8.2 GHz



Model 1255
8.2 - 12.4 GHz

Figure 1-1. ACTO Units.

CHAPTER 2 — INSTALLATION

2-1. *INITIAL INSPECTION*

As soon as the ACTO unit is received unpack it carefully, saving the packing materials if possible. Verify that the ACTO is intact and as ordered. Inspect the instrument for any physical damage. If damage of any nature is found a claim should be filed immediately, with the shipper.

As soon as possible the ACTO should be installed in a counter and given a thorough electrical inspection. The test given in Chapter 5 is recommended for this purpose. Should the ACTO fail to operate properly or fail to meet specification, immediately contact your nearest Systron-Donnor representative.

NOTE

Unauthorized repair or soldered parts replacement to any Systron-Donner instrument during the Warranty Period may void the warranty. Do not attempt repair or soldered parts replacement without prior authorization from the Service Manager of your nearest Systron-Donner representative or from the factory. (The only exceptions are plug-in printed circuit cards and tubes which may be replaced on a unit exchange basis.)

2-2. *STORAGE AND RESHIPMENT*

Environmental conditions during storage and shipment should be limited as follows:

a. Maximum Temperature 185° F (85° C)

b. Minimum Temperature -69° F (-55° C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable custom packaging on short notice.

a. If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb sq. inch bursting strength) or wooden box to house the instrument.

b. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

c. Use plenty of packing material around all sides of the instrument and protect the front panel with cardboard strips.

d. Seal the package with strong tape or metal bands. Mark with "Delicate Instrument."

e. Refer to the warranty page at the rear of this manual and check with Systron-Donner field office for shipping instructions. All correspondence should refer to an instrument by model number and the full serial number.

2-3. *INSTALLATION*

The three ACTO plug-ins are compatible with Systron-Donner Model 1017, 1018, 1037, 1037 Frequency Counters. Installation is accomplished by the following steps.

1) Remove the plug-in or blank module presently installed in the counter by turning the locking knob counterclockwise at least two full turns then pulling the plug-in out by its handle. Generally a firm pull will be required to unseat the connector at the rear of the plug-in.

2) Place the ACTO in the plug-in receptacle and push it in until its panel is flush with the front panel of the counter. A firm push may be necessary to seat the connector at the rear of the ACTO.

3) Lock the ACTO in place by turning the locking screw clockwise until it is tight. Check by giving the ACTO's handle a firm pull. If the ACTO is not locked, back off on the locking screw and tighten it again.

2-4. *POWER AND COOLING REQUIREMENTS*

All power and cooling required by the ACTO is furnished by the counter in which it is installed. Installation of the ACTO will increase the power requirement of the counter by 10 watts.

CHAPTER 3 — OPERATION

3-1. INTRODUCTION

The operation of any of the three ACTO plug-ins is extremely simple. Once the counter has been set up, operation of the ACTO is completely automatic. The counter setup instructions given in this manual will be brief and functional in nature; for detailed operational procedures on the counter, please refer to the Instruction Manual for the applicable counter model number.

As operation of all ACTO units is identical, the operation procedures will not be referenced to any particular ACTO model. The only precaution to be observed is the frequency range of the ACTO. Frequencies considerably above or below the normal range of any ACTO model may give false readings. Input signal amplitudes should also be observed closely. Although, typically, the ACTO will measure signals considerably below its rated sensitivity of 100 mv rms signals below that level can give false readings. Similarly signals with too much amplitude (above 0.5 v rms) will give false readings and above 2 v rms may damage the instrument.

3-2. OPERATION

Before making a measurement with the ACTO, set the counter controls as follows: (Refer to Figure 3-1 for a graphic measurement procedure).

1) Plug the counter into a 115 vac, 60 Hz source and turn the POWER switch ON.
2) Set the FUNCTION switch to RATE.
3) Set the TIME BASE switch to the setting commensurate with the desired resolution. Resolution is easily determined as it is directly proportional to the time base setting; thus, a time base setting of 1 (sec) gives 1 Hz resolution, a setting of 10^{-1} (0.1 sec) gives 10 Hz resolution, 10^{-2} (0.01 sec) 100 Hz resolution, etc. Up to 10^{-5} (10 μsec) 100 K Hz resolution.

> **NOTE**
>
> The 10^{-6} and 10^{-7} Time Base settings cannot be used with the ACTO. Incorrect readings will result if these settings are used.

4) Set the RANGE switch to the HET (Heterodyne) position.
5) Set the DISPLAY control (concentric with the time base switch) for the desired time of display. The control will vary the time the reading is displayed from approximately 0.1 to 5 seconds or infinite.
6) Set the LEVEL control to mid position.
7) Set the STORAGE switch (located on the rear panel of the counter) as desired. In the ON position only answers will be displayed. The readout display will change only when the answer changes. In the OFF position readout cycling prior to the answer will be displayed as well as the answers.
8) Set the COUNTER-R F switch on the ACTO to R F.
9) Set the SENSITIVITY control on the ACTO to the maximum counterclockwise position.
10) Connect the signal to be measured to the RF input on the ACTO.
11) Rotate the SENSITIVITY control in the clockwise direction until the +1 MC light comes on, indicating that the ACTO is locked to the input frequency.
12) Read the input frequency on the counters indicators. If the answer is unstable or missing adjust the level control on the counter until a stable reading is obtained.

> **NOTE**
>
> Unless the input frequency is extremely stable a certain amount of jitter is to be expected in the last one or two indicators.

A normal measurement will require steps 10, 11 and 12 only. A simple check to determine whether operation is correct is to place the COUNTER-RF switch in RF, note the indication, then place the FUNCTION switch in the TEST position and note the indication. When the two indications are multiplied they should equal the input frequency.

3-3. MEASUREMENT OF SIGNALS WITH AM

The procedure for measuring signals with amplitude modulation is the same as that used for measuring CW signals. The ACTO will measure an AM signal so long as the rms signal level at the point of maximum modulation is at least 100 mv rms (-7 dbm). Thus for a signal at the 500 mv rms (+7 dbm) maximum usable level, 80% modulation would be the maximum modulation the ACTO would tolerate.

3-4. MEASUREMENT OF SIGNALS WITH FM

Frequency modulated signals may be measured with the ACTO if specifications are closely observed. The measurement procedure is the same as that previously described. The frequency displayed will be the center frequency of the FM signal.

To determine whether it will measure a particular FM signal use the following specification:

0.1% frequency deviation at a 60 Hz deviation rate.

Derated at 6 db per octave as the deviation rate increases.

As an example for a 1 GHz signal with a 60 Hz deviation rate, maximum frequency deviation would be 100 K Hz; if the deviation rate increased to 120 Hz, maximum frequency deviation would be 50 K Hz. If the amount of FM is excessive the ACTO will break lock and the +1 MC light will extinguish. (Erratic answers may be displayed.)

3-5. *MEASUREMENT CONSIDERATIONS*

When making any measurement with the ACTO it is important that the following operating techniques be used. Even though, normally, a signal may be measured simply by applying it to the ACTO, carelessness can cause false readings or damage to the instrument. It is, therefore, mandatory that proper techniques be used.

1) Be sure that the input signal is within the range of the ACTO, both in frequency and amplitude. Proper amplitude is especially important. Amplitude must be between plus and minus seven dbm. Signals above 2 volts rms will damage the instrument.

2) Always start with the sensitivity control fully counterclockwise (least sensitive) and then turn it clockwise until the +1 MC light comes on indicating lock-on. If this procedure is not followed it is possible for the ACTO to lock onto the second harmonic of the input and display a false reading.

3) When making AM or FM measurements observe the specifications of the ACTO closely. Percentage of modulation and deviation rate, respectively, are the key specifications.

4) If the reading is missing or jittery even though the ACTO is locked on (illumination of the +1 MC light indicates lock-on) adjust the LEVEL control on the counter. This adjustment is normally not necessary, but should be checked if the reading appears jittery or is missing.

3-6. *OPTION W OPERATION*

The W option allows the ACTO to be used as a plug-in to the Model 5245L, Electronic Counter, manufactured by the Hewlett-Packard Corporation.

Setup and operation of this counter-plug-in is nearly identical to that of the standard Systron-Donner units.

To make a measurement with the W Option proceed as follows:

1) Turn the SAMPLE RATE control for POWER ON.

2) Turn the SENSITIVITY switch to PLUG-IN.

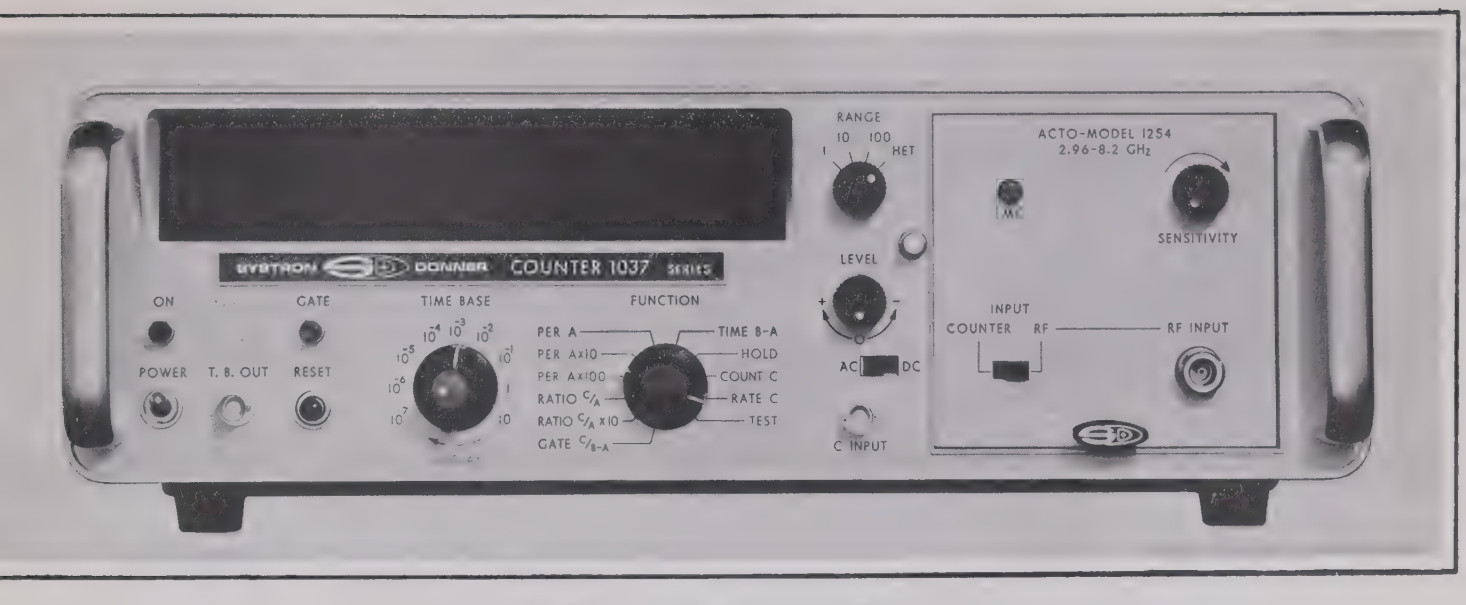
3) Set the TIME BASE switch as described in paragraph 3-2, step (3).

4) Set the FUNCTION switch to FREQUENCY.

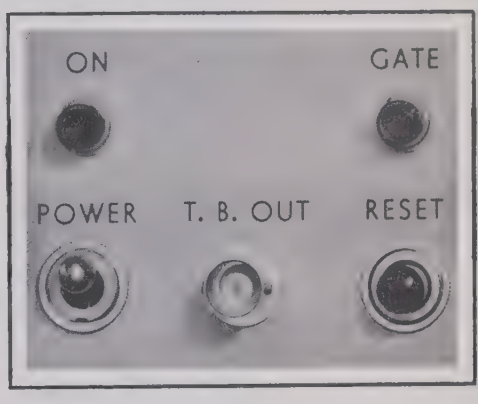
5) Set the STORAGE ON-OFF switch (located on the rear panel) to ON (see paragraph 3-2, step (6) for detailed discussion).

6) Perform the remainder of the measurement as outlined in paragraph 3-2, step (7) to 3-2, step (11) or as shown in the last five steps of the photographic sequence.

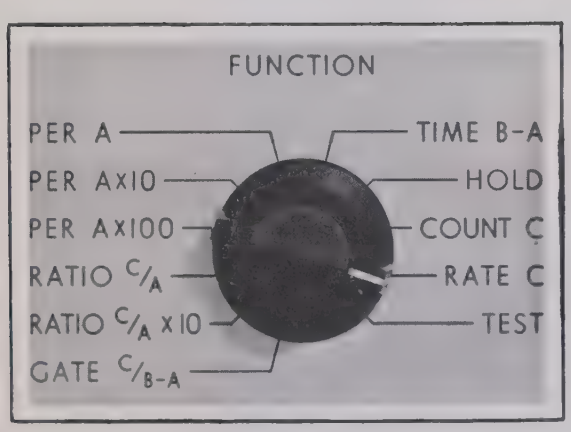
Figure 3–1. ACTO Measurement Procedure (Sheet 1 of 3)



Model 1037 Counter with ACTO



1. Plug **COUNTER** in and turn **POWER** switch on.

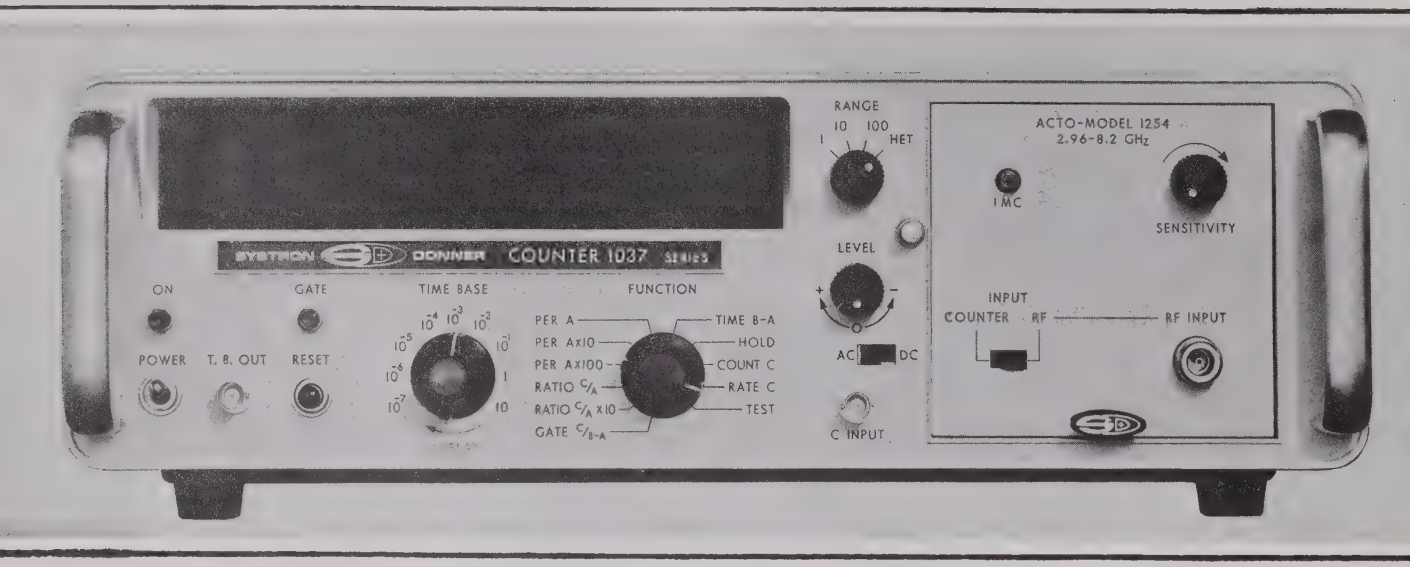


2. Set **FUNCTION** switch to **RATE**.

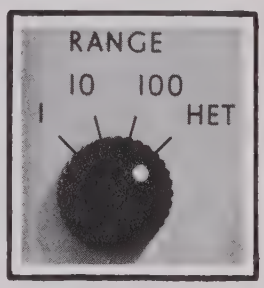
3. Set **TIME BASE** switch for desired resolution (see para. 3.2.2 for detailed discussion).

   DO NOT USE 10^{-6} OR 10^{-7} TIME BASE POSITIONS

Figure 3–1. ACTO Measurement Procedure (Sheet 2 of 3)

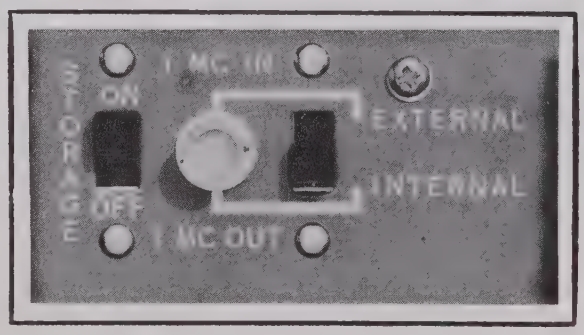


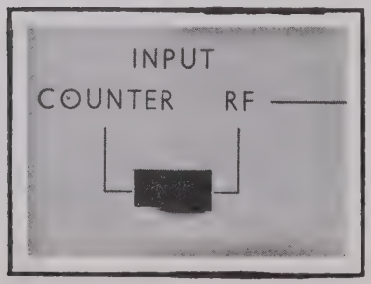
4. Set the **RANGE** switch to **HET**.



5. Set the **LEVEL** Control to the Mid-Position (see para. 3.2.12 for a detailed discussion).

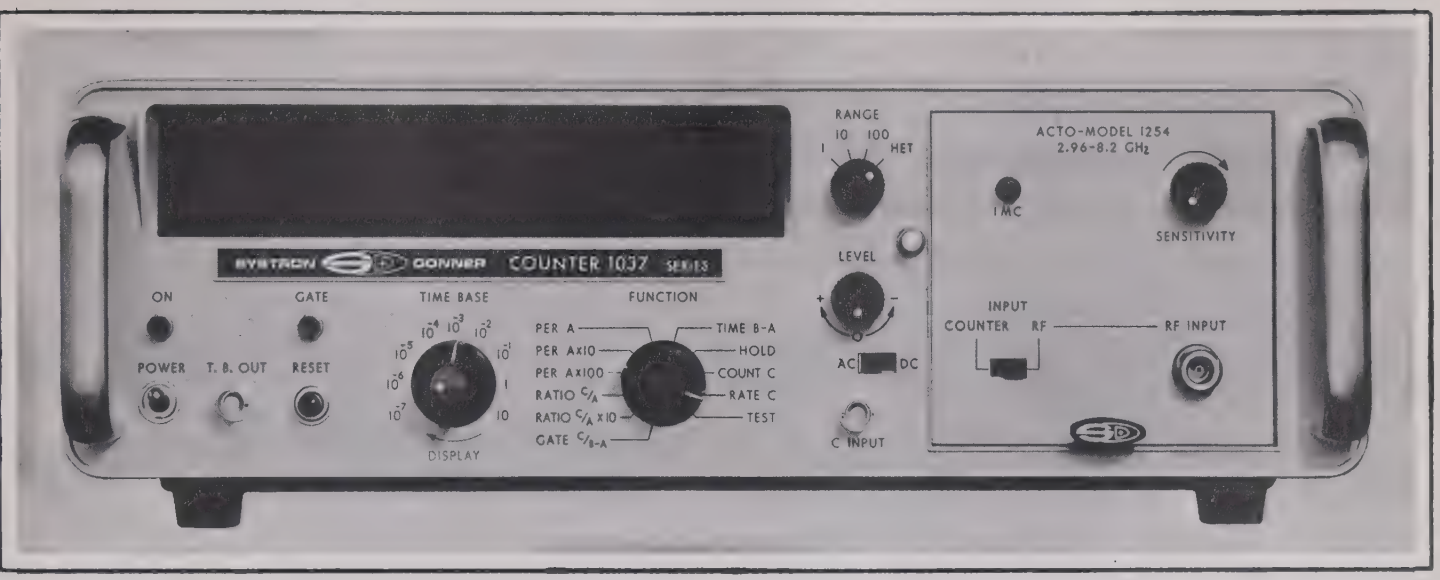
6. Set the **STORAGE ON-OFF** switch to **ON** (see para. 3.2.6 for detailed discussion).



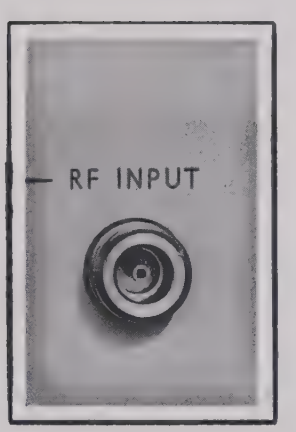


7. Set the **COUNTER-RF** switch to **RF**.

Figure 3–1. ACTO Measurement Procedure (Sheet 3 of 3)

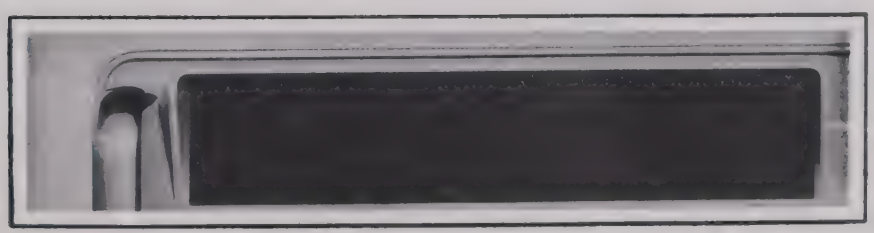


8. Set the SENSITIVITY control maximum counterclockwise.



9. Connect INPUT SIGNAL to the ACTO (type N connector).

10. Turn the SENSITIVITY control clockwise until the 1 MC Light comes on.



Read Answer

NORMALLY ONLY THE STEPS ON THIS PAGE WILL BE REQUIRED.

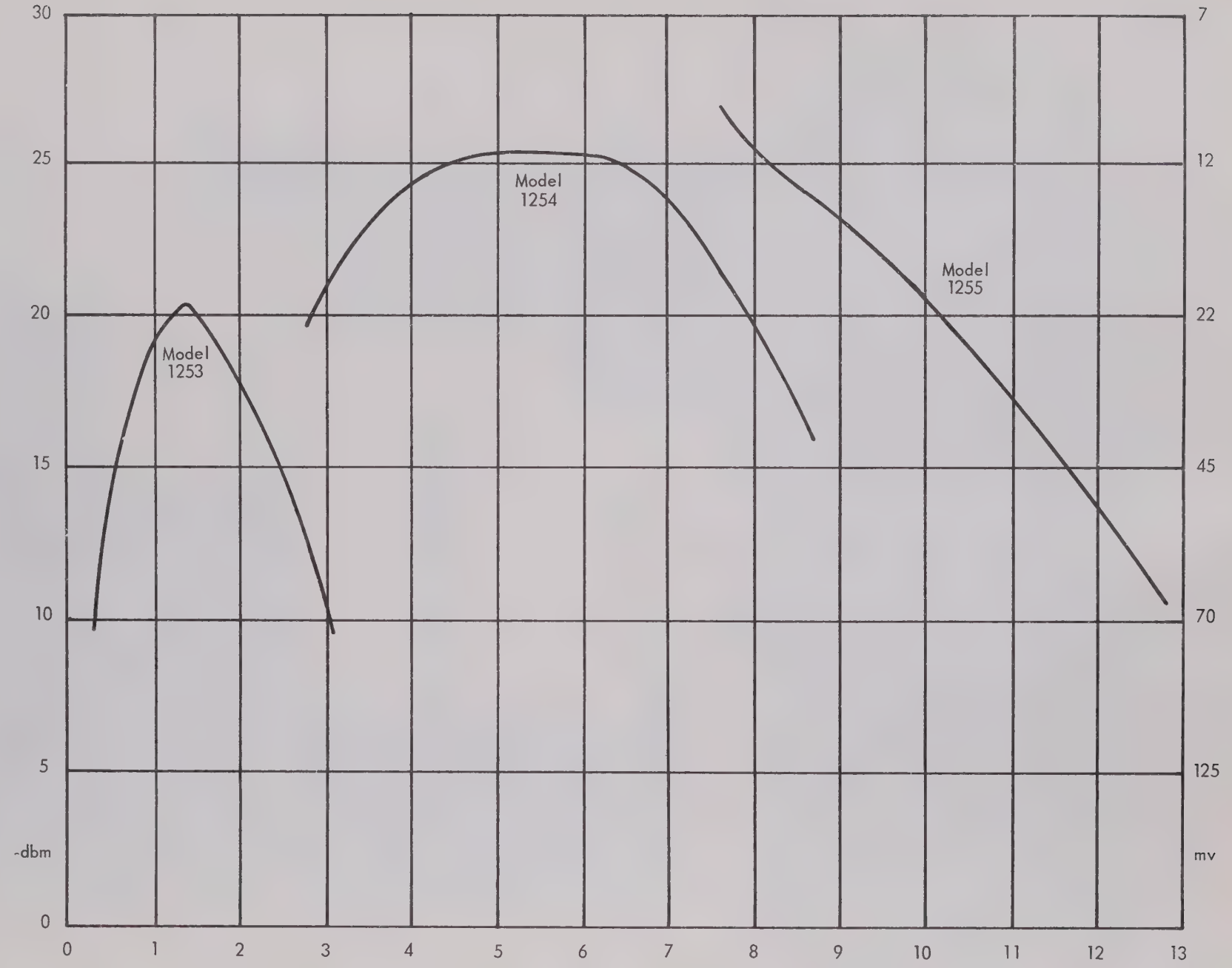


Figure 3–2. ACTO, Typical Sensitivity

CHAPTER 4 - THEORY OF OPERATION

4.1 GENERAL INFORMATION

The Automatic Computing Transfer Oscillator (ACTO®) Plug-ins extend the frequency measuring range of 50 or 100 MHz counters to 0.3 to 12.4 GHz. Using the transfer oscillator technique, the ACTO matches a harmonic of its own oscillator to the unknown input frequency. The unit then computes the harmonic number and expands the counter time base so that the counter reads out the input frequency minus one megahertz. A phase-lock circuit insures that counter accuracy is maintained (±1 count ± time base stability).

4.1.1 SCOPE OF DISCUSSION

The following discussion covers the theory of operation of three models in the ACTO series: Models 1253, 1254, and 1255. If the description of a circuit or function is not qualified with a model number, the description may be assumed to apply to all three models. The discussion is presented on three levels: the basic block diagram (Section 4.2), the functional block diagram (Section 4.3), and the schematic diagrams (Section 4.4). All of the diagrams are included in this chapter.

NOTE

In some cases, the value of a particular component may vary from model to model. The same is true of the operating frequency of tuned circuits. Since these parameters do not affect the theory of operation, the differences are not reflected in the text. Reference should be made to the schematic diagram or parts list of the particular model in question for component values, and to Chapter 5 for alignment values.

4.1.2 TRANSFER OSCILLATOR OPERATION

An understanding of the conventional transfer oscillator frequency measuring technique is essential to the discussion of ACTO operation. For this reason, the basic techniques are outlined here.

In a manually-operated transfer oscillator, a harmonic generator typically produces at least the first ninety-nine harmonics of the output frequency of a tuneable oscillator. The harmonics are mixed with the unknown input frequency, and the oscillator is tuned manually until the input frequency is matched by a harmonic. When this coincidence has been achieved, usually by obtaining a zero beat on a built-in CRT, the operator multiplies the oscillator frequency by the harmonic number. The oscillator frequency is usually displayed on the counter, and the harmonic number, on the oscillator tuning control.

Operator skill is required in the selection of the proper harmonic. Additionally, time is consumed both in the original measuring operation, and in the verification process which normally follows. The ACTO eliminates the need for operator skill and greatly reduces the time required. The answer normally appears on the counter less than one second after the input is applied to the ACTO. The operator need only add one megahertz to the readout to determine the input frequency.

4.2 BASIC BLOCK DIAGRAM

Figure 4-1 is a basic block diagram of the ACTO. The diagram relates the basic functions within the unit, but is not meant to show all of the functions or signal paths.

4.2.1 OPERATIONAL DESCRIPTION

The unknown input frequency feeds a mixer assembly that also receives two inputs from a swept oscillator. One of the oscillator output signals is at the oscillator fundamental frequency; the other is shifted by one kilohertz. The oscillator fundamental frequency is also sent to the counter. The dual outputs of the mixer are sent to the lock and harmonic number (N) channels.

The lock channel controls the sweep of the oscillator. The sweep is halted when some harmonic of the oscillator frequency is phase-locked one megahertz below the unknown input frequency. The locked-on condition is attained by rotating the ACTO SENSITIVITY control until the "+1MC" light is ON. When the locked on condition is achieved, the oscillator output is gated into the counter.

The N channel processes a signal which has a frequency of 1 MHz ±N (1 KHz). The signal is amplified and the 1 MHz component removed.

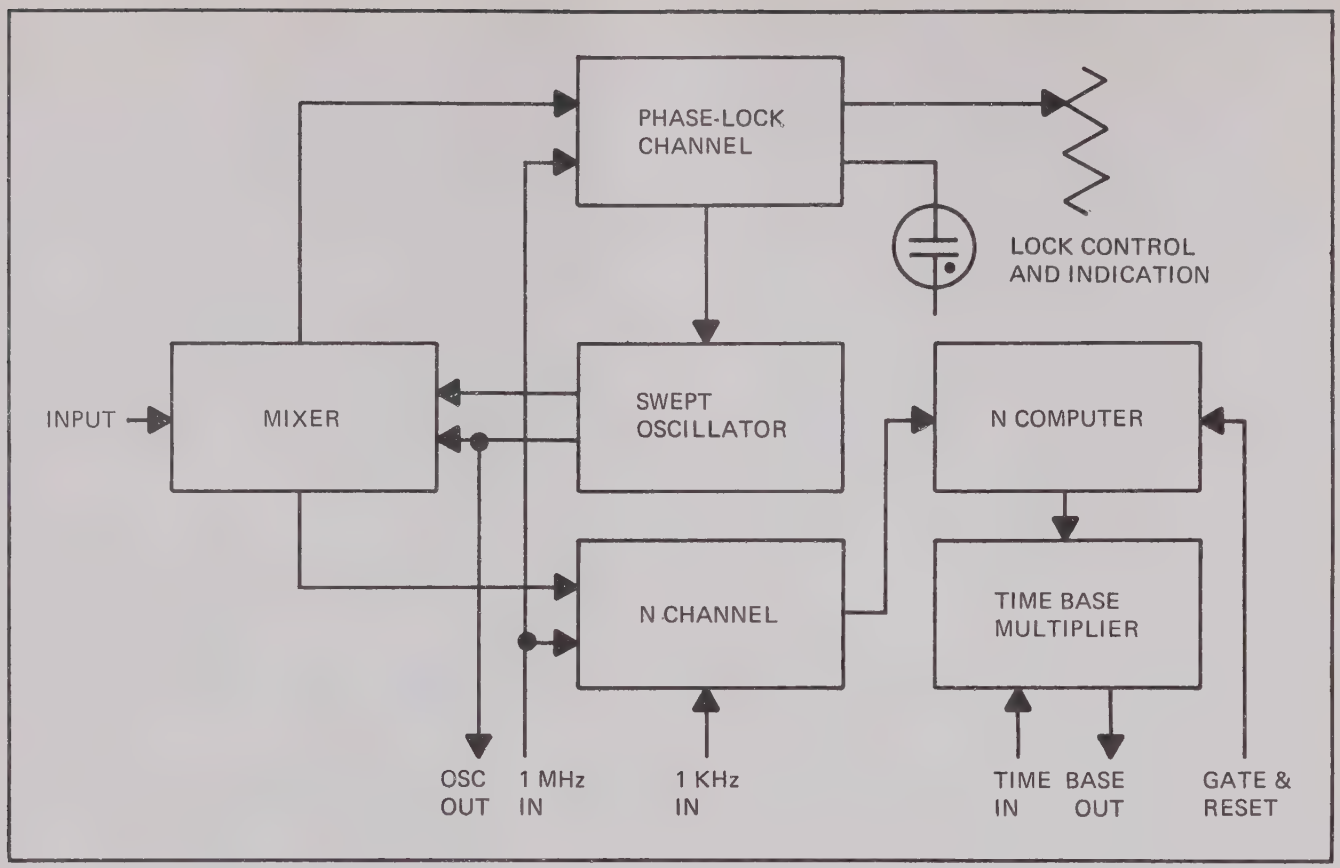


Figure 4-1 Basic Block Diagram

The remaining signal is shaped and sent to the N computer.

The N computer effectively divides its signal input by one kilohertz to produce a pulse train containing N pulses. The counter time base period is expanded (multiplied) by the harmonic number, and the oscillator frequency is counted during this time period. The result is a counter readout one megahertz below the input frequency.

The counter in which the plug-in is installed provides GATE and RESET signals to the N computer, and precise one kilohertz and one megahertz frequencies to other circuits in the ACTO. The counter also supplies all necessary voltages and ground references needed by the ACTO.

4.3 FUNCTIONAL BLOCK DIAGRAM

Figures 4-2a and b are the functional block diagrams of the ACTO units. The diagrams use a combination of blocks, electronic symbols and digital logic to show the relationship between circuits in the ACTO. Each block or symbol has been labelled to indicate its function or major component. In addition, each block contains, in its upper right-hand corner, a number. These numbers are keyed on the diagram and relate to the physical subassembly on which the circuit appears. The numbers correspond to the J-numbers of the connectors in which the subassemblies are mounted. Circuits on the mixer subassemblies are coded with "M", rather than a number.

The blocks are connected with lines that indicate both signal flow paths and sensing lines. When a line represents an interconnection between subassemblies, pin numbers on the respective connectors are shown. Heavy lines are used to show major signal paths in the two channels.

In the discussion that follows, a block with several inputs or outputs may be described more than once. It should also be remembered that the functions of the two channels take place simultaneously for all practical purposes, rather than sequentially as depicted here. References to "Figure 4-2" without an alphabetic designator concern circuits that appear on both sections of the drawing.

4.3.1 INPUT CIRCUITRY

The unknown RF input entering the ACTO

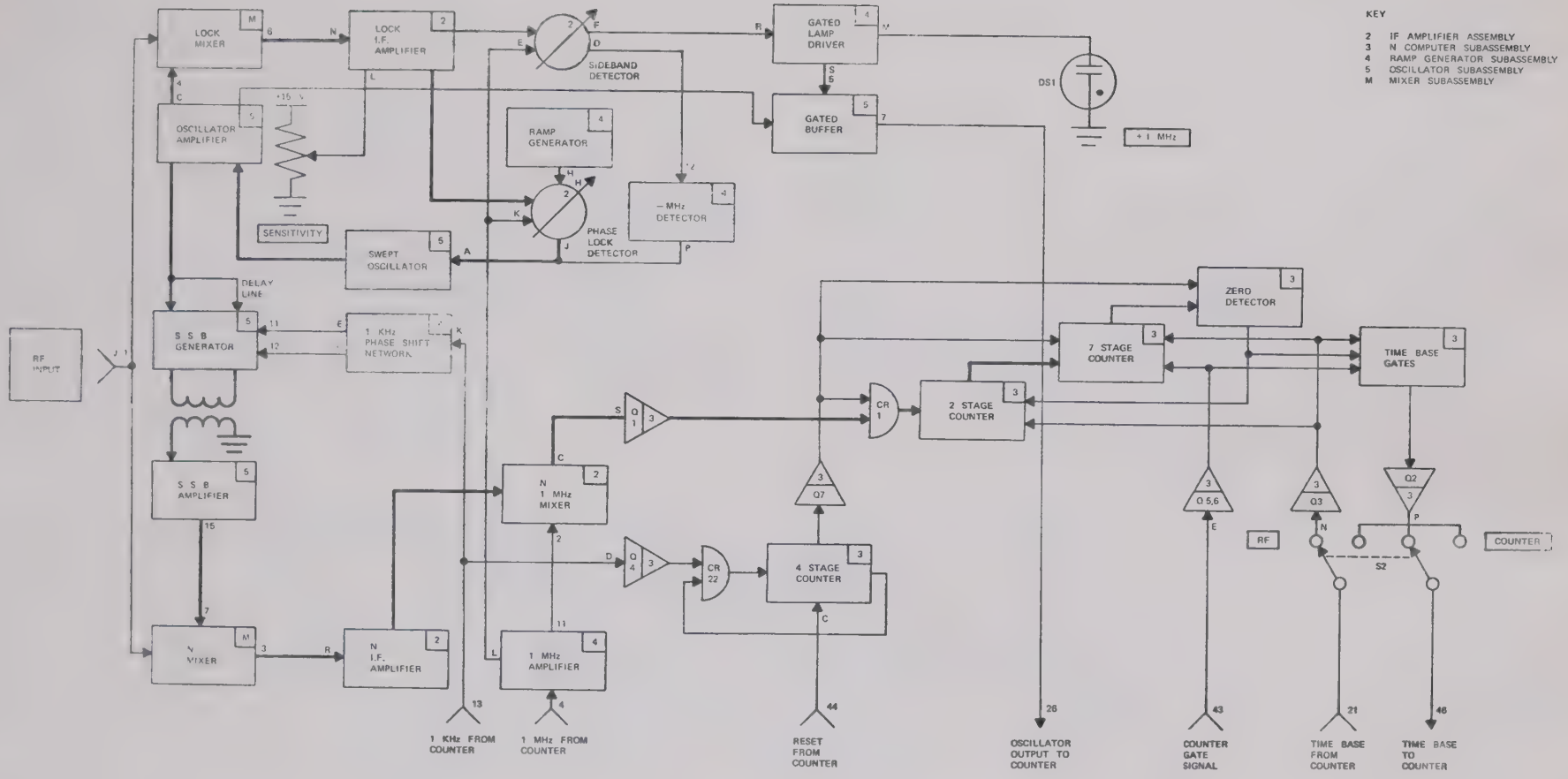


FIGURE 4-2a MODEL 1253 FUNCTIONAL BLOCK DIAGRAM

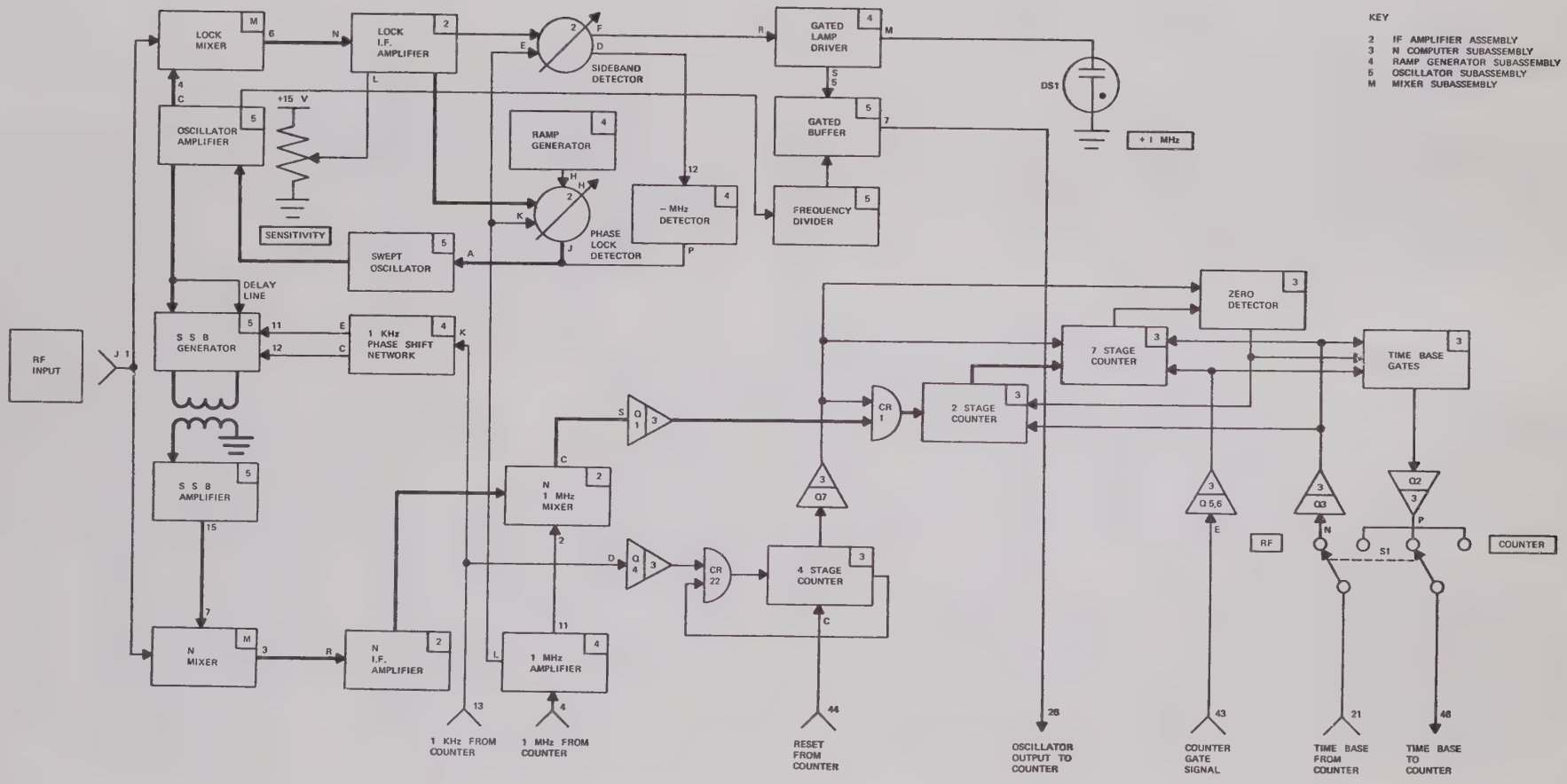


FIGURE 4-2b MODELS 1254 and 1255 FUNCTIONAL BLOCK DIAGRAM

through front-panel Jack J1 (left side of Figure 4-2) is split and applied to the mixers of the lock and N channels. The other mixer inputs are the output of the ACTO swept oscillator. One signal from the oscillator output amplifier feeds the lock channel mixer directly. Another signal feeds two parallel inputs of a single-sideband generator.

The single-sideband generator receives two pairs of inputs. One pair of inputs comes from the swept oscillator. One of the oscillator signals, however, passes through a delay line that shifts its phase ninety degrees. The other pair of inputs is derived from the precise one-kilohertz signal from the counter. A phase-shifting network develops two one-kilohertz signals, one shifted ninety degrees with respect to the other.

The output of the single-sideband generator is a frequency separated from the oscillator fundamental by one kilohertz. The separation may be either additive or subtractive without affecting circuit operation, since the N computer uses the absolute value of the difference frequency. The generator output is transformer-coupled to an amplifier, and then coaxially coupled to the mixer.

4.3.2 MIXER SUBASSEMBLY

The blocks in Figure 4-2 coded "M" represent the mixer subassembly. While different types of subassemblies are used in the different models, each performs the same basic functions: dividing the unknown input into the two channels, generating harmonics of the swept oscillator outputs, and mixing the harmonics with the unknown signal.

The fundamental signal from the oscillator amplifier passes through a harmonic generator located in the lock channel mixer, and is mixed with the unknown signal to provide an output to the lock channel. The amplified output of the single-sideband generator feeds the harmonic-producing circuitry for the N channel. Subsequent discussion will show that the signal frequency at the N mixer output is displaced from the lock channel mixer output by N kilohertz.

4.3.3 ONE MEGAHERTZ AMPLIFIER

A precise one megahertz signal from the oscillator in the counter is necessary to the operation of both the lock and N channels. Since the source impedance requirements of the two channels differ widely, the incoming signal is buffered before distribution. The output to the N channel represents a high-impedance source while the output to the lock channel detectors has a low source impedance.

4.3.4 LOCK CHANNEL INTERMEDIATE FREQUENCY AMPLIFIER

The Lock Channel IF Amplifier is a multi-stage amplifier broadly tuned to one megahertz. The IF amplifier processes the mixer output signal for delivery to two of the detector circuits. The front-panel SENSITIVITY control adjusts the gain of this amplifier.

4.3.5 DETECTOR CIRCUITS

There are three circuits in the lock channel that serve as detectors. Each measures at least one parameter of its input signal (magnitude, polarity, phase relationship) and, under a predetermined set of conditions, produces a controlling output.

The phase-lock detector compares the output of the IF amplifier with the precise one-megahertz signal from the counter. The IF amplifier output frequency is the difference between the unknown input frequency and the oscillator harmonics. This is accomplished by modifying the output of the ramp generator, which passes through this detector before it reaches the oscillator.

One output of the sideband detector is a gate signal. In the detector, the IF amplifier output is rectified and the resulting voltage used to control two gates. Since the IF amplifier is tuned to one megahertz, only at one megahertz will the signal be of great enough magnitude to produce a rectified voltage sufficient to enable the gates. The sideband detector also compares the output of the IF amplifier to the one-megahertz signal. This time, however, the IF amplifier output has been shifted ninety degrees. As a result, the polarity of the phase comparator output is a function of whether the ACTO is locked on to the sideband above or below the unknown input frequency. This polarity-dependent output is sent to the -1 MHz detector.

The -1 MHz detector insures that phase lock occurs with an oscillator harmonic below the input frequency. The input to this detector is the signal from the phase comparator in the sideband detector. The output from the -1MHz detector modifies the signal that is sweeping the oscillator. If the phase-lock detector tries to lock on to a harmonic above the input frequency, the signal from the -1MHz detector forces the oscillator to continue sweeping.

4.3.6 GATED LAMP DRIVER, GATED BUFFER, AND FREQUENCY DIVIDER

When lock is achieved with an oscillator harmonic one megahertz below the input frequency, the gate output of the sideband detector opens the gate in the lamp driver. Until this time, the driver circuit has been shunting the neon-bulb indicator; now the bulb is permitted to light. The gate signal passes through the lamp driver to a gate in the oscillator amplifier output. With lock achieved, the output of the oscillator is permitted to pass to the counter. In the Models 1254 and 1255, the swept oscillator frequency is above the range of 50 MHz counters, but within the direct counting range of 100 MHz counters. To make the 50 MHz counters compatible, a divide-by-two circuit is added between the oscillator amplifier and the gated buffer. This frequency division is compensated for in the N computer of these models.

4.3.7 N CHANNEL SIGNAL FREQUENCY

Understanding the circuitry in the N channel, particularly in the N computer, depends on understanding its signal frequency components. Since the N channel frequency is controlled by the lock channel, the following discussion begins with lock frequency determination.

If we designate the fundamental frequency of the swept oscillator as F, then any output of the lock channel harmonic generator is

① $N(F)$

where N is the harmonic number. If we designate the unknown input as X; and the mixer produces the algebraic difference, $|D|$, between its two inputs; then the statement for the lock channel mixer output is

② $N(F) - X = |D|$.

But, the lock channel detectors restrict the value of D to one megahertz, and the relationship of X and N (F) to $X < N(F)$. Therefore, statement ② becomes

③ $X - N(F) = 1\ \text{MHz}$

The output of the oscillator is increased by one kilohertz before introduction into the N channel harmonic generator, and becomes

④ $F + 1\ \text{KHz}$

Any output from the N channel harmonic generator is, therefore,

⑤ $N(F + 1\ \text{KHz})$,

which may be rewritten

⑥ $N(F) + N(1\ \text{KHz})$.

The N channel mixer provides the algebraic difference between statement ⑥ and the unknown input, X:

⑦ $X - [N(F) + N(1\ \text{KHz})]$,

which may be rewritten

⑧ $X - N(F) - N(1\ \text{KHz})$.

But, from statement ③ we see that

⑨ $X - N(F) = 1\ \text{MHz}$

Therefore, the output of the N channel mixer is

⑩ $1\ \text{MHz} - N(1\ \text{KHz})$.

Statement ⑩ defines the frequency sent to the N channel IF amplifier.

4.3.8 N CHANNEL INTERMEDIATE FREQUENCY AMPLIFIER

The N channel IF amplifier is similar to its counterpart in the lock channel. The two-stage amplifier is broadly tuned to one megahertz, but no sensitivity control is provided. The 1 MHz - N (1KHz) signal is amplified and sent to the one megahertz mixer. The mixer combines the N channel signal with the precise one megahertz signal from the counter. The one megahertz signals cancel, to produce a mixer output of N (1 KHz). This signal is shaped and sent to the N computer.

4.3.9 N COMPUTER GENERAL OPERATION

The N computer performs two functions: It extracts the harmonic number from the N kilohertz input signal, and it expands the counter time base by N. The N computer operates in the binary, or two-valued, number system. The "building blocks" of the computer are buffers, gates and counters. The buffers prepare computer input and output signals for use in other circuits. The gates are control devices that permit or deny passage of a signal as a function of their controlling inputs. The counters are

strings of flip-flops, or bistable circuits, that serve in a two-valued system as counting and storing devices.

Some basic characteristics of binary digital counters must be understood before continuing the discussion of the N computer. Each stage of a counter is a flip-flop, internally connected so that one cycle of its input signal causes one change of state (one-half cycle) of its output signal. Each stage changes state at approximately the same point on its input waveform. Figure 4-3 shows the output signal from each stage of a three-stage counter.

Figure 4-3 illustrates two important characteristics of a binary counter: The counter divides its input frequency by 2^S, where S equals the number of stages (a three-stage counter divides by $2^3 = 8$); and each stage of the counter holds one state for

$$\frac{2^S}{2}$$

periods of the counter input signal (the third stage remains in either state for

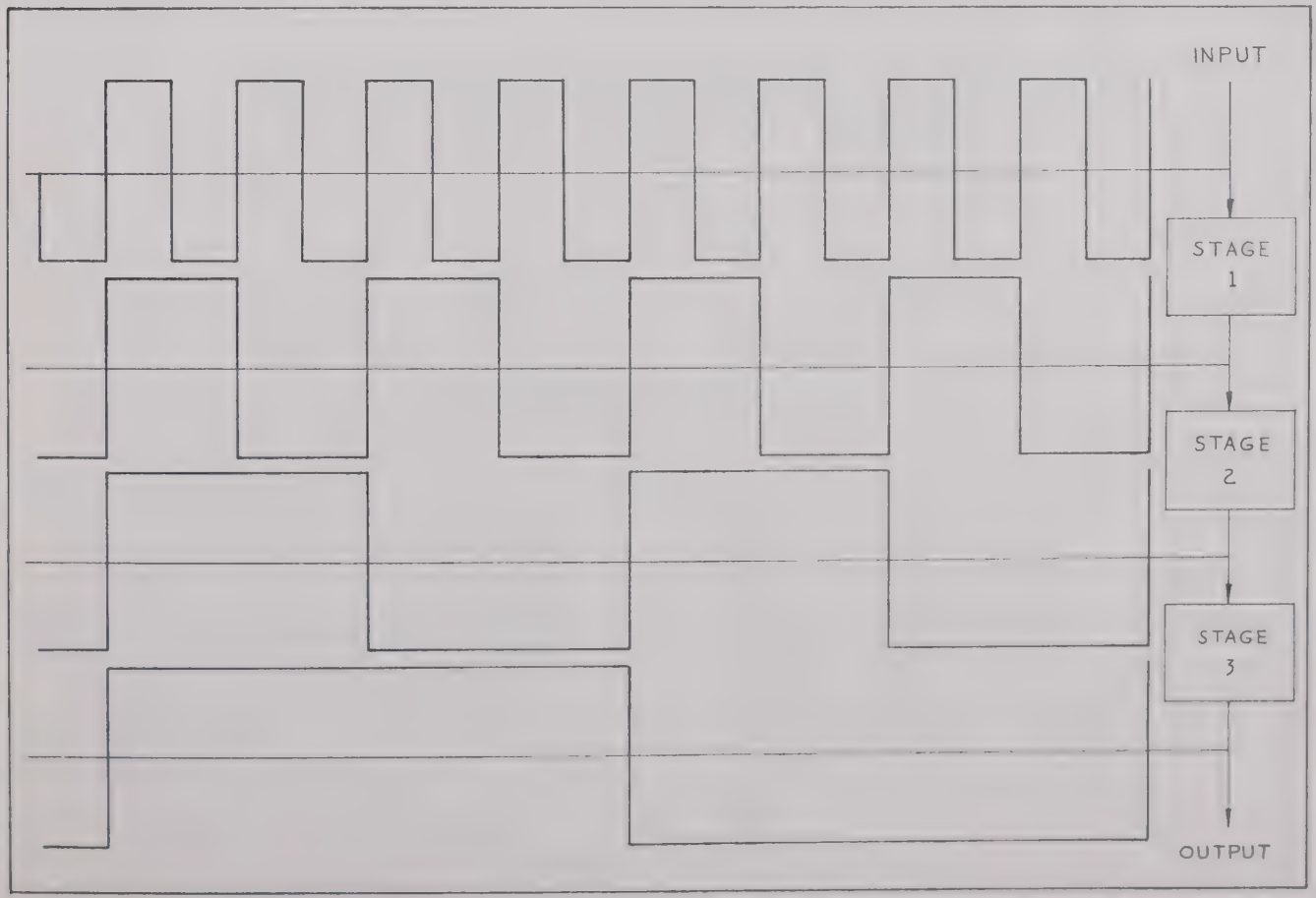
$$\frac{2^3}{2} = \frac{8}{2} = 4$$

periods of the input signal).

There are three counters in the computer, containing respectively seven (or eight) stages, four stages, and two stages. To reduce confusion, they will be referred to in subsequent discussions as "counter-7", "counter-4", and "counter-2". The term "counter" without a numeral will refer to the instrument in which the ACTO is mounted.

An eight-stage counting device is used in the Model 1255 because the largest possible harmonic number in that model (125) approached the maximum capacity of a seven-stage counter (128). Operation of counter-7 in the Model 1255 is otherwise unchanged. Counter-7 is used to count and hold N during a delay built into the counter between the RESET and GATE signals. After the hold period, counter-7 counts down the harmonic number to time the time base expansion. To perform these functions, counter-7 must be able to count in both directions.

The method used to extract the harmonic number from the N kilohertz input signal takes advantage of the availability of a precise one kilohertz signal from the counter. Inspection will show that N cycles of the input signal must occur during the one millesecond period of the one kilohertz signal. If, therefore, the input



signal is gated into counter-7 during a one millisecond period, counter-7 will contain the harmonic number. A problem arises, however if a counter-7 input pulse coincides with a gate transition. Under these conditions, counter-7 might ignore the input, resulting in an error in N. Since any such error would be reflected as an inaccuracy in the counter readout , it cannot be tolerated. The following discussion shows how this error is eliminated.

4.3.10 ERROR ELIMINATION

The operation of the N computer is initiated by a counter RESET signal that resets the fourth stage of counter-4. An output of this fourth stage has, until this time, been inhibiting a gate in the input path to counter-4. The signal input to this gate is the buffered one kilohertz signal from the counter. With the gate now open, counter-4 counts until its fourth stage sets and again closes this gate. This process is shown in Column 1 of Table 4-1.

During the counting period of counter-4, the third stage produces an enabling signal for

$$\frac{2}{2} = \frac{2^3}{2} = \frac{8}{2} = 4$$

periods of the input signal. Since the input to counter-4 has a one millisecond period, this enabling signal exists for four milliseconds. If this signal were used to gate the N kilohertz signal into counter-7, the result would be a count of 4N. To provide the proper input to counter-7, the buffered N kilohertz signal is gated into counter-2 by the buffered 4 ms forward gate signal. Counter-2 will divide this input by four.

If the first stage counter-2 is preset to the negative state, the first counted pulse must always cause a negative-to-positive transition. Since the second stage can only trigger on the positive-to-negative transition, this first count is always ignored. By presetting the second stage to the positive state, a countable output on the second pulse is assured.

Figure 4-4 diagrams the conditions set forth in the two preceding paragraphs. Line 1 shows a hypothetical N kilohertz input signal, where N = 5. Line 2 shows the 4 ms forward gate signal occuring in a worst-case phase match with Line 1. Lines 3 and 5 show two possible outputs from the first stage of counter-2. On Line 3, both input pulses occurring at the gate transitions have been counted. On Line 5, neither has been counted. Lines 4 and 6 show

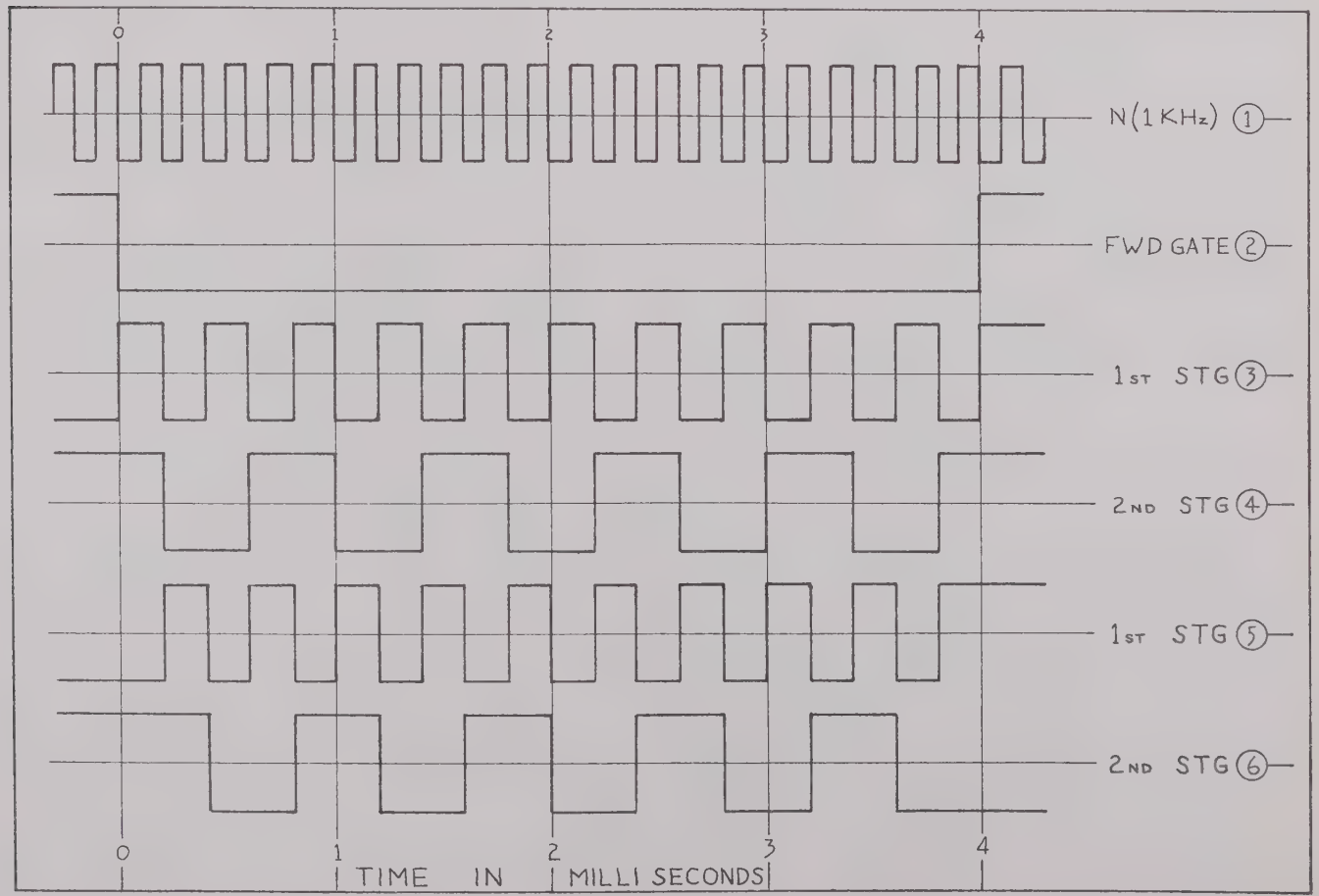


TABLE 4-1

FOUR-STAGE COUNTER TRUE OUTPUTS

	COLUMN 1					COLUMN 2			
STAGE	1	2	3	4		1	2	3	4
STATE									
0	0	0	0	0	= After Reset				
1	1	0	0	0		1	0	0	1
2	0	1	0	0		0	1	0	1
3	1	1	0	0		1	1	0	1
4	0	0	1	0		0	0	1	1
5	1	0	1	0		1	0	1	1
6	0	1	1	0		0	1	1	1
7	1	1	1	0		1	1	1	1
8	0	0	0	1	= Gate Closed				

STATES shown in Column 1 occur during normal cycle of counter 4.

STATES shown in Column 2 might occur at turn-on but would exist only until receipt of first reset pulse.

that in either case, the output contains five positive-to-negative transitions which will serve as the input to counter-7.

4.3.11 COUNTER-7 OPERATION

Counter-7 has two sets of input and controlling signals. One input signal is the train of N pulses from counter-2. The control signal for this input is the 4 ms forward gate signal from counter-4. This set of signals enables counter-7 to count in the forward direction. The other input signal is the time base signal from the counter. The control signal for this input is a reverse gate signal derived from the buffered counter GATE signal. This set of signals enables counter-7 to count backwards.

The ability to count in both directions is derived from the interstage gates in counter-7. These gates are shown in Figure 4-5. The forward gates connect the normal output of each stage to one of two parallel inputs on the next stage. The backward gates connect the inverted output of each stage to the remaining parallel input of the next stage.

The counter GATE signal is normally the length of one time base period, and occurs approximately forty milliseconds after the RESET pulse. (This is a fixed delay and is a function of circuitry internal to the counter.) The GATE signal is normally enabled by one time base pulse and disabled by the next. Since it is during this period that the input to the counter is counted, this is the period that must be expanded. To accomplish this, the time base pulse that would disable the GATE signal must be prevented from returning to the counter. This function is performed by the time base gates.

4.3.12 TIME BASE GATES AND ZERO DETECTOR

The counter time base is buffered as it enters the N computer. In the Models 1254 and 1255, a divider circuit halves the time base frequency before it is used in the computer. This doubling of the time base period compensates to the halving of the swept oscillator frequency as discussed in Subsection 4.3.6. When the counter GATE signal is turned on, it disables the time base return path to the counter. The GATE signal enables the backward interstage gates, and the time base pulses drive counter-7 as it counts backwards through the harmonic number.

When counter-7 reaches zero, the zero detector, which has until this time been disabling three gates, switches to an enabling output. One of these gates is in the time base signal return path to the counter. The next time base pulse disables the GATE signal and counts counter-7 down to -1. The next time the computer counts the harmonic number, the zero detector is prevented from operating on the forward count by the forward gate signal. (Counter-7 actually only counts up to N-1.) This last time base pulse also passes through the counter-2 reset gates to preset counter-2 as discussed in Subsection 4.3.11.

With the GATE signal disabled, the counter ceases its count of the swept oscillator frequency. (In the Models 1254 and 1255, the counter only received half of the oscillator frequency, but in these models the time base period was doubled.) The counter readout now indicates the ACTO input frequency minus one megahertz.

4.4 SCHEMATIC DIAGRAM

The description of the schematic diagram is organized around the schematic of the Model 1253. Additional circuitry in the Models 1254 and 1255 is discussed as it occurs. Schematics for all three models are included in this chapter, but circuitry common to all three is diagrammed only once. The schematics may be cross-referenced to the functional block diagram (Figure 4-2) by using the subassembly J-numbers and interconnecting pin designators.

4.4.1 SCHEMATIC BLOCK DIAGRAM

Figures 4-6a and 4-7a show the frame-mounted components and the relationship between the major subassemblies. Across the bottom of the diagram are shown the terminals of connector P1. The three units are electrically identical with the exception of the mixer. Figure 4-6a includes a schematic of the dual harmonic mixer assembly used in the Model 1253. The Models 1254 and 1255 use coaxial 3 db couplers as power splitters and separate mixers for each channel.

4.4.2 MIXERS

The dual harmonic mixer subassembly in the Model 1253 mixes the unknown RF input with the fundamental and shifted fundamental outputs of the swept oscillator, each in a separate channel. The mixer is of the strip-line type, that is, some of its elements are derived from distributed effects in the printed

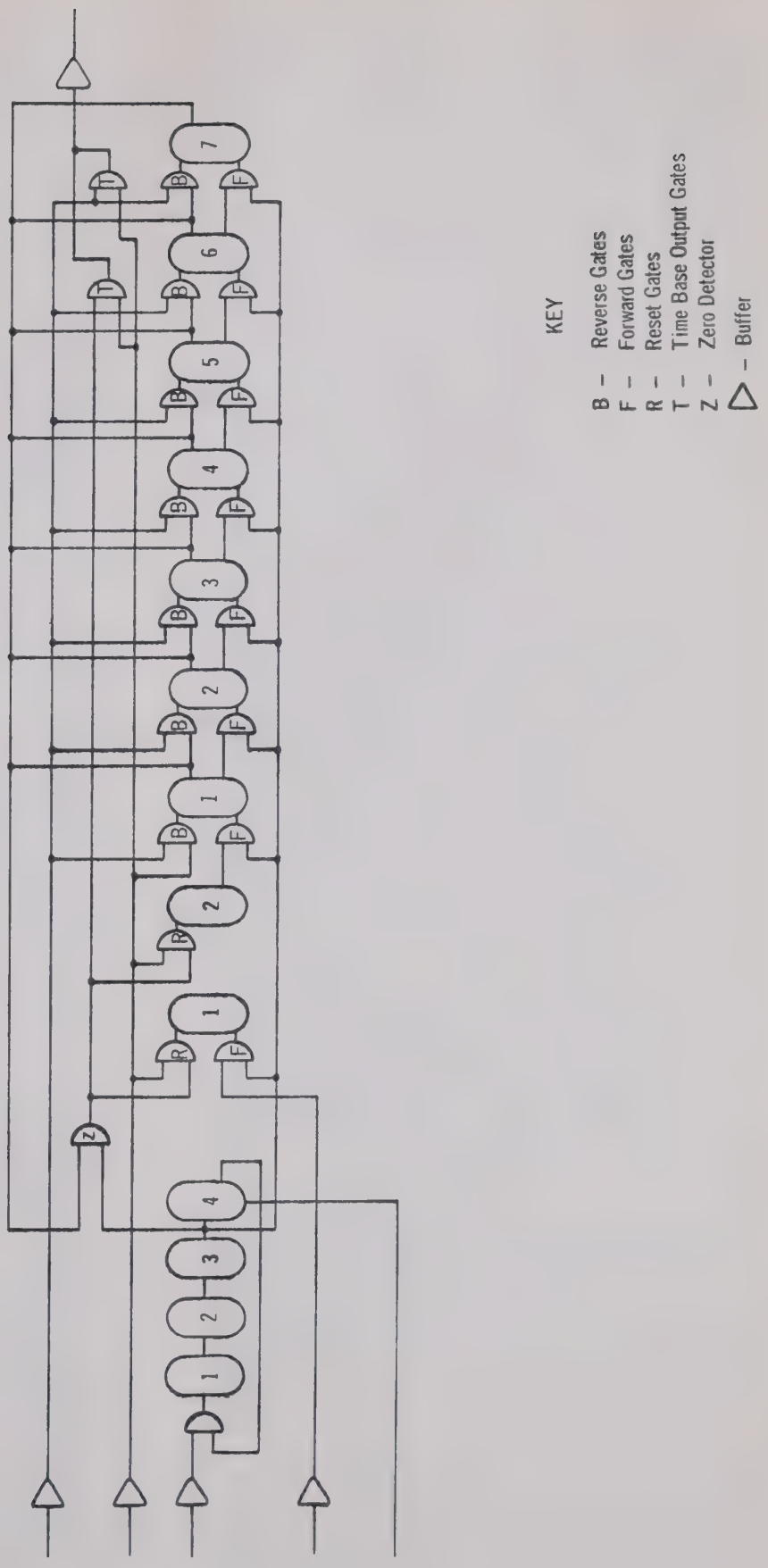


FIGURE 4 - 5 N COMPUTER LOGIC DIAGRAM

circuitry of the mixer, rather than from discrete components. The mixer is mounted on the frame of the ACTO immediately behind the front panel. Since there are two identical channels, only one is described here.

The unknown RF input feeds the 10 db pad, RF2. This resistive element, with its counterpart in the other channel, serves the dual frunction of presenting an approximately standard input impedance to the incoming signal and isolating the channels from each other. The pad is a resistor "T" with one arm connected to the input, the other arm connected to inductor L2, and the base of the "T" connected to ground. Rather than a discrete component, inductor L2 is an isolated finger of printed circuitry. A feed-through to the ground plane at the base of the finger insures the presence of a ground reference at that point. The harmonic and mixer diodes are connected to the other end.

Diode CR4 is the harmonic generator. The input to the cathode of CR4 is the fundamental frequency from the swept oscillator. The diode conducts normally during one half of each incoming cycle, and begins to conduct during the other half. However, at some point near the beginning of this second half cycle, the rectifying capability of the diode takes over and its output rapidly returns to zero. In this "step recovery", harmonics of the incoming frequency are generated. A small ferrite bead, E2, is placed on the input lead of CR4 to suppress any spurious response.

Diode CR3 is the mixer. At its cathode it receives harmonics from CR4 and the unknown input frequency. The resultant output is difference frequencies between these two which are sent to the lock channel. The diodes are discrete components, but capacitors C3 and C4 occur as distributed effects in the connectors and printed circuits.

The mixers in the other two models are of a more conventional nature. A separate power splitter terminates the incoming signal and divides it between the two channels. The two mixers are mounted immediately behind the front panel. Different mixers and hybrids are used in each model because of the differing frequency requirements.

4.4.3 FRAME- AND PANEL-MOUNTED COMPONENTS

The primary frame-mounted components are the connectors and the ±15 volt power supply components. Connector P1 is located at the base of the rear panel. All connections to and from the counter are made through this connector. The subassembly connectors, J2 through J5, are mounted on the main frame of the ACTO. Resistors R2 and R4 are mounted on connector J5 and serve as termination impedances for their respective oscillator output cables. Capacitor C3 is mounted on connector J2 as a power supply by-pass on the sensitivity control.

The positive and negative 30 volt power supplies from the counter are used to develop the ±15 volts needed in the ACTO. Components C1 and R5 perform this function for the negative supply, as do C2, R6, and CR1 for the positive. In addition, inductors L1 and L2 are interposed in the ±15 volt lines to the oscillator and IF amplifier subassemblies to prevent carry-over of signal frequencies.

On the front panel are mounted the input jack, J1, and input selector, S21, as well as the lock control, R1, and lock indicator, DS1. Resistor R3 supplies current for the neon after it fires.

4.4.4 INTERMEDIATE FREQUENCY AMPLIFIER SCHEMATIC

The intermediate frequency amplifier subassembly contains the IF amplifier for both the lock and N channels, the N channel one megahertz mixer, and the lock channel detectors. Physical construction of the subassembly is oriented toward reduction of electromagnetic interference. Prior to installation in the ACTO, the printed circuit board is mounted on a metal cover that shields its "wire" side. The printed circuitry on the component side of the board is etched only for component attachment, two signal leads, and a voltage input. The remaining twelve pins on the "component" side of connector J2 are grounded to the chassis. A shield is also provide between the N channel and lock channel components.

Inputs to the board include the buffered one megahertz signal from the counter and the ±15 volt power supplies. Since the two channels require different source impedances for their one megahertz signal, two different inputs are provided. The negative 15 volt supply is used only in the lock channel circuitry.

4.4.5 N CHANNEL IF AMPLIFIER

The N channel IF amplifier receives a signal from the N channel mixer at Pin R. The signal frequency is equal to one megahertz plus the harmonic number multiplied by one kilohertz [1 MHz + N (1 KHz)] . Potentiometer

R13 is used to adjust the bias on the mixer diode. Amplifier stages Q1 and Q2 and their associated circuitry are broadly tuned to one megahertz. This rejects some of the unwanted harmonics produced in the mixer.

The impedance-matched one megahertz signal is injected on the base of Q3 and produces a difference frequency at Q3 of N(1 KHz). This signal passes through a low pass filter composed of L3 and C6, 17, and 18 which rejects frequencies above 300 KHz. Test point TP1 permits observation of the N channel waveform before it is shaped for the N computer. The test point is accessible with the shield cover installed. Transistors Q4 and Q5 form a Schmitt trigger that shapes the output of the IF amplifier-mixer before its introduction into the harmonic number computer. Phase modulation may be present on the signal, but will not affect operation of subsequent circuitry.

4.4.6 LOCK CHANNEL IF AMPLIFIER

The IF amplifier in the lock channel operates similarly to the amplfier in the N channel. Potentiometer R36 biases the mixer diode through the input at Pin N. Amplifier stages Q6 and Q7 are broadly tuned to one megahertz and have their base bias, and therefore their gain, controlled by the front-panel SENSITIVITY control. Transistors Q8 and Q9 operate as a differential limiter with each stage supplying a detector. Resistor R31 in the base-collector circuit of Q8 provides DC feedback to stabilize the limiter.

4.4.7 DETECTORS

The phase-lock detector receives three input signals: precision one megahertz at Pin K, the output of the ramp generator at Pin H, and the output of the lock channel IF amplifier capacitively coupled from Q9. The single output of the detector at Pin J is the modified ramp to the swept oscillator.

As long as the intermediate frequency at the center tap of the primary of T1 is not one megahertz, an imbalance exists in the two output legs of the primary. This imbalance allows Q10 to turn on sufficiently to pass the ramp signal. When the IF matches the one megahertz on the secondary, the two legs balance. Now, Q10 continues to provide the necessary current to hold the oscillator at this frequency. It should be noted here that the ramp generator is a current, rather than voltage, source.

The sideband detector, composed of T2 and its supporting components, operates similarly to the basic elements in the phase-lock detector. The signal at the center tap of the primary, however, is phase-shifted before it reaches Q11. As a result, when lock is achieved, the polarity of the voltage at Pin D is a function of the phase relationship between the IF and 1 MHz reference. This signal feeds the -1MHz detector on the ramp generator subassembly.

4.4.8 N COMPUTER SCHEMATIC

The basic theory of N computer operation is discussed in Subsection 4.3.7 - .12, and a logic diagram of the computer is shown in Figure 4-5. The following discussion covers the implementation of the theory in the hardware. The three N computers operate in a similar manner. In the Models 1254 and 1255, a time base frequency divider is added to compensate for the division of the swept oscillator frequency in those models. The seven-stage counter in the Models 1253 and 1254 is increased to eight stages in the Model 1255. This prevents overflowing the counter at frequencies only slightly above the upper specified limit of the ACTO (12.4 GHz).

Both discrete and distributed components are used in the N computer flip-flop circuitry, a schematic of which is shown beside the main schematic. The resistive and capacitative elements are deposited on a sub-strate that forms the top of the container for the conventional transistors. The diodes are also discrete components and are mounted on the bottom of the container. The connections shown within the dotted lines on the flip-flop schematic are internal to the element. All other connections are made on the printed circuit board in which the element is mounted.

4.4.9 FOUR-STAGE COUNTER

Counter-4 is composed of flip-flops FF11 through FF14, and produces the four millisecond forward gate signal when triggered by the one kilohertz signal from the counter. The one kilohertz signal at Pin D is buffered by Q4 and fed to CR22 which acts as a gate. The controlling input to the gate is the false output of FF14 fed back through R34. As a result, counter-4 runs until the output of FF14 inhibits CR 22. During this period, the false output of FF13 is true for four milliseconds (see Table 4-1) and is used as the forward gate signal. The counting cycle of counter-4 is initiated by a RESET signal from the counter entering the subassembly at Pin C and changing the state of FF14, thus reopening gate CR22.

4.4.10 TWO-STAGE COUNTER

Counter-2 is composed of flip-flops FF1 and FF2. With gate CR1, Counter-2 performs the multiply/divide operation needed to eliminate the possibility of a one-count ambiguity (see Subsection 4.3.10) in the input to counter-7. The incoming N channel signal at Pin S is buffered by Q1 and sent to gate CR1. The controlling signal on the gate is the forward gate signal developed by counter-4 and buffered by Q7. Counter-2 is reset to a specific condition by the signals at Pin 10 of FF1 and Pin 3 of FF2. The source of these reset signals will be discussed in subsequent paragraphs.

4.4.11 SEVEN-STAGE COUNTER

Counter-7 is composed of flip-flops FF3 through FF9 (and FF15 in the Model 1255). Gates in the signal paths between the stages permit counter-7 to count in either direction. The forward interstage gates are diodes CR5, 6, 8, 10, 12, 14, 16, and 34, and are controlled by the forward gate signal. The backward interstage gates are diodes CR4, 7, 9, 11, 13, 15, 17, and 35, and are controlled by the GATE signal from the counter. In the forward counting mode, counter-7 is triggered by the output of counter-2. When the forward gates are disabled, counter-7 stores the value N-1 awaiting the reverse count.

The reverse gate signal is derived from the GATE signal developed by the counter. This counter GATE is enabled by a counter time base pulse approximately forty milliseconds after the RESET pulse that initiated the counter-4 cycle. The next time base pulse would normally disable the GATE signal, resulting in a signal period equal to the time base period. During this time, the unknown input will be counted. In this case, the unknown input is the swept oscillator fundamental frequency (or half the fundamental frequency in the Models 1254 and 1255). To obtain an accurate readout, this frequency must be multiplied by the harmonic number (or twice the harmonic number). This multiplication is achieved by expanding the GATE period.

To prevent two consecutive time base pulses from enabling and then disabling the GATE, the time base signal is routed into the ACTO through buffers Q6 and Q5 and, once enabled, is used to block the return path of the next time base pulse at gate CR20. With the counter 7 backward gates enabled by this same GATE signal, the time base pulses now count down the N-1 value stored in counter-7.

In Models 1254 and 1255, FF10 is interposed in the time base path after Q3. Time base pulses trigger FF10, alternately enabling and disabling gate CR32. As a result, only every other time base pulse passes the gate to trigger counter-7.

4.4.12 ZERO DETECTOR AND TIME BASE GATES

The reverse gate signal disables gate CR20, preventing the next time base pulse from returning to the counter and disabling the GATE signal. (As long as GATE remains on, the counter continues counting.) The time base pulses count down counter-7 until a count of zero is reached. At zero, the zero detector composed of Q8 and diodes CR24 through CR30 (and CR36 in Model 1255) produces an enabling output.

The enabling output from the zero detector opens gates CR2, CR3, and CR19. The next time base pulse passes through these gates to preset counter-2 and disable the GATE signal. This same time base pulse counts counter-7 to a "-1" state. This accounts for counter-7 only reaching a maximum count of N-1. Since the GATE signal has been enabled for N (or, in Models 1254 and 1255, 2N) periods, the beginning state of counter-7 is of no consequence. The zero detector is prevented from operating on the forward count by the forward gate signal at the base of Q8.

4.4.13 RAMP GENERATOR SCHEMATIC

The ramp generator subassembly is common to all three models of ACTO. The subassembly contains the ramp generator, one kilohertz phase shifting network, one megahertz buffer, gated lamp driver, and -1 MHz detector. Each circuit has its own input and output connections. Only the ±15 volt power supplies are common to all five circuits.

The ramp generator provides the changing voltage that varies the frequency of the swept oscillator. Transistors Q11 and Q12 form a one-shot, or monostable multi-vibrator circuit. When Q12 comes into conduction (representing the unstable state of the one-shot), the output at Pin H is approximately -15. Resistor R51 now represents a current source. When the one-shot returns to its stable state, this source begins a linear charge of a capacitor on the oscillator subassembly. When the ramp reaches a predetermined point, Q10 switches, developing a

pulse that triggers the one-shot and restarts the cycle. Resistor R45 in the B2 base circuit of Q10 is nominally 1 KΩ. This resistor is factory-selected to compensate for differences in switching potential of individual 2N1671B transistors.

The one kilohertz phase shifting network produces two sinusoidal one kilohertz signals with a ninety degree phase difference between them. The one kilohertz signal from the counter is an unsymmetrical square wave. The RC network between Q14 and Q15 represents a "notch" filter that will not pass the 1 KHz portion of the input signal. All of the other harmonics are routed back to the base of Q14 as negative feedback. The resulting one kilohertz sine wave is coupled through C28 to the base of Q16. Q16 is a phase-splitter, with outputs taken from both its collector and its emitter. The uninverted signal at the emitter feeds Pin E. The inverted signal at the collector is shifted ninety degrees in the coupling network, C20 and R78, and at Pin C, exhibits a ninety degree shift from the Pin E signal.

The tuned one megahertz amplifier serves two purposes: It compensates for waveshape variations in the input signal, and it provides impedance-matched outputs to the two ACTO channels. The RC network in the base circuit of Q18 compensates for some variations in the incoming waveform. In addition, the LC network in the collector circuit aids in providing a clean sinusoidal output. The signal at Pin L drives the low-impedance secondaries on the lock channel phase detector transformers. The low impedance reduces the possibility of any signal frequencies being coupled back to this amplifier. The signal at Pin 11 drives the slightly higher input impedance of the N channel one megahertz mixer.

The gated lamp driver controls the ACTO front-panel "1 MC" lamp (indicating that lock has been achieved, and the operator must now add one megahertz to the counter readout). The gate signal at Pin R is developed in the lock channel sideband detector by rectifying the channel IF. The indicator lamp and its positive power supply are connected to the collector of Q21. When the ACTO is not locked on, Q21 is turned on and the indicator turned off. This is because the potential at the collector is below the firing potential of the neon bulb. When lock is achieved, the signal at the base of Q19 turns that transistor off. This allows the collector of Q21 to rise until the neon fires. The gate signal is coupled out of Pin 5 to the oscillator subassembly.

Transistor Q23 serves as the -1 MHz lock detector. Accurate interpretation of the counter readout depends on lock occurring with some swept oscillator harmonic one megahertz below the unknown RF input. Since the phase-lock detector senses only the absolute value of the difference frequency, a second detector with one phase-shifted input is used to develop a sideband-dependent signal (see Subsection 4.4.7).

One output of the sideband detector depends upon the phase relationship between the phase-shifted IF and the buffered one megahertz signal. This output appears at Pin 12 of the -1 MHz detector. If lock has occurred on at additive (rather than subtractive) sideband, Q23 is turned on and the signal at Pin P overrides the ramp and pulls the oscillator off lock.

4.4.14 OSCILLATOR SCHEMATIC

The oscillator subassembly contains the swept oscillator, its output amplifier and gated buffer, and the single sideband generator and its output amplifier. The physical construction of the subassembly is similar to that of the IF amplifier subassembly. The component side of the board is completely plated and etched only for component mounting and a minimum of signal leads. Shielding perpendicular to the board isolates related components. When the unit is installed in the ACTO, it is mounted in a metal shield cover.

Inputs to the board include the ±15 volt power supplies on Pins 10 and 13, and the one kilohertz signal from the phase shift network (see Subsection 4.4.13) on Pins 11 and 12. The oscillator also receives the modified ramp from the phase-lock detector on Pin A, and the gated buffer receives its controlling input from the sideband detector at Pin 5. There are two outputs from the subassembly: the oscillator fundamental frequency to the lock channel mixer at Pin C, and the same frequency shifted one kilohertz at Pin 15. This latter output feeds the N channel mixer.

The swept oscillator is a modified Colpitt's oscillator with a center frequency of 33 megahertz in the Model 1253 and 99 megahertz in the Models 1254 and 1255. In these latter two models, the oscillator frequency is divided in half before being gated into the counter. (This makes these models compatible with the 50 MHz counters.) Aside from the frequency divider and some individual component differences required for circuit tuning, all three oscillator subassemblies operate similarly.

The oscillator tank circuit is composed of coil T2, and diodes CR2 and CR3 (or capacitor C26). The diodes act as variable capacitors, changing the tank frequency as the voltage at their anodes changes. The output of the ramp generator, as modified by the phase-lock detector, charges capacitor C33, and thus varies the voltage on the diodes. As the voltage rises linearly from approximately -14 volts to +8 volts, the oscillator frequency varies over a 3.5 megahertz range across the center frequency. The sweep occurs at a 10 Hertz rate and appears as a sawtooth, rather than a triangular, waveform. This is accomplished by returning to the negative potential by switching a one-shot in the ramp generator, rather than by a linear discharge of C33.

Three separate uses are made of the fundamental frequency from the swept oscillator: as an input to the harmonic generator in the lock channel mixer, an input to the single-sideband generator that serves as the N channel frequency shifter, and as an input to the counter. Since it is not desireable to load the oscillator directly, and some degree of isolation is required between the loads, an output amplifier is provided.

The output to the lock channel harmonic generator is taken at Pin C after two stages of tuned amplification, Q6 and Q7. A 47Ω resistor (shown on schematic block diagram) terminates the oscillator-mixer coax to reduce any signal reflections that may occur. The isolated test point at Pin 2 on J5 is provided to allow measurement of the output signal for tuning purposes.

The output to the single-sideband generator is taken after one additional stage of amplification, Q8. A short length of coaxial cable routes the 0.5 volt peak-to-peak signal from C37 to C18. At this point, the signal is split to provide the two inputs required by the generator. The signal path from C18 to the junction of R15 and C13 is a coaxial delay line that imparts a 90 degree phase shift to the signal. The length of delay line depends on the oscillator frequency. (Since the propagation rate is approximately one inch every 140 picoseconds, the Model 1253 requires 54 inches and the other two models, 18 inches. This produces a ninety degree shift.)

In the Models 1254 and 1255, the oscillator frequency is divided by two before being sent to the counter. The division is accomplished with a flip-flop composed of Q10 and Q11. The oscillator output is introduced at the emitters of Q9 and Q12. These two transistors steer the incoming signal to the base of either Q10 or Q11 to switch the flip-flop. The output, at half the input frequency, is taken at the collector of Q10. In the Model 1253, an RC coupling network replaces the flip-flop.

The oscillator output to the counter at Pin 7 is turned on only when lock is achieved. The gate signal at Pin 5 is developed by a rectifier associated with the sideband detector. When Q14 is turned off, there is no source of emitter current for Q13. As a result, even though Q13 is driven, there is insufficient output. When the gate turns Q14 on, Q13 passes the oscillator output to the counter. The minimum acceptable output would be a 100 mv rms signal.

4.4.15 SINGLE-SIDEBAND GENERATOR

The single - sideband generator shifts the swept oscillator ouput frequency by one kilohertz for use in the harmonic number (N) channel. (Whether the shift is additive or subtractive is of no consequence. The operation of subsequent circuitry depends on the magnitude and not the direction of the shift.) The generator is essentially a pair of balanced modulators with their output vectorially added. The frequency shift is accomplished by phase rotation of the swept oscillator output at a one kilohertz rate. The result of this advancement or retardation of the RF input is a one kilohertz frequency shift.

The single-sideband generator receives two pairs of inputs. One pair of input signals is the fundamental frequency of the swept oscillator. One of these signals, however, passes through a delay line (see Subsection 4.4.14) and lags the other signal by ninety degrees. The other pair of inputs are developed by the one kilohertz phase shifting network described in Subsection 4.4.13. The one kilohertz signal at Pin 12 of the single sideband generator lags the signal at Pin 11 by ninety degrees. (The phase relationship between the RF and modulating signals has no affect on the output.)

The output from the single sideband generator is taken from the secondary of tuneable transformer, T1. This inductive coupling reduces the effects of output amplifier loading on the generator. The frequency at the primary is more easily understood if its separate signal components are analyzed individually.

Ignoring the presence of the other modulator and any modulating signal temporarily, if an RF signal is introduced at the connected emitters of Q1 and Q2, identical signals will

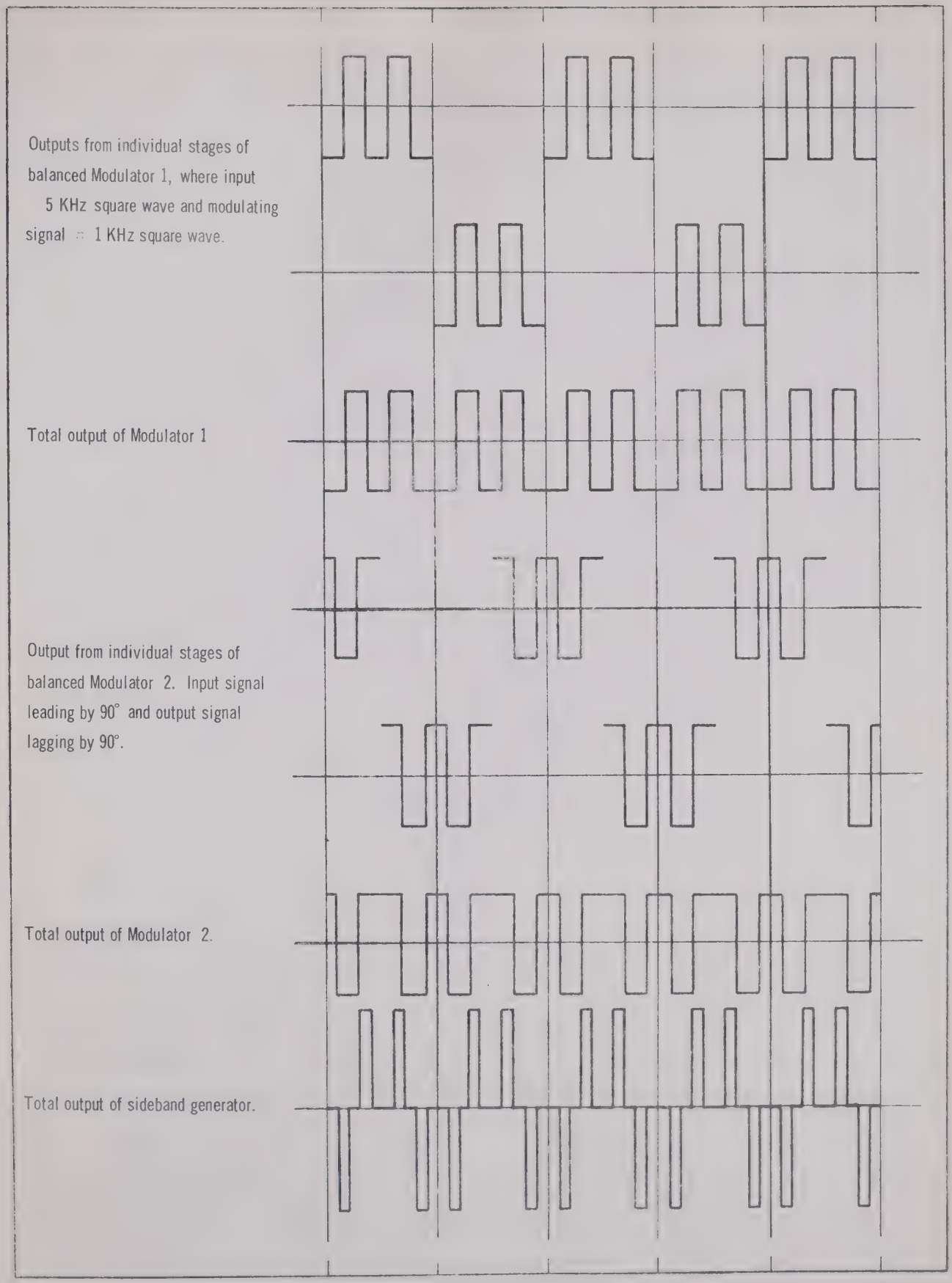

Outputs from individual stages of balanced Modulator 1, where input 5 KHz square wave and modulating signal = 1 KHz square wave.
Total output of Modulator 1
Output from individual stages of balanced Modulator 2. Input signal leading by 90° and output signal lagging by 90°.
Total output of Modulator 2.
Total output of sideband generator.

FIGURE 4 - 8 SINGLE - SIDEBAND GENERATOR OPERATION

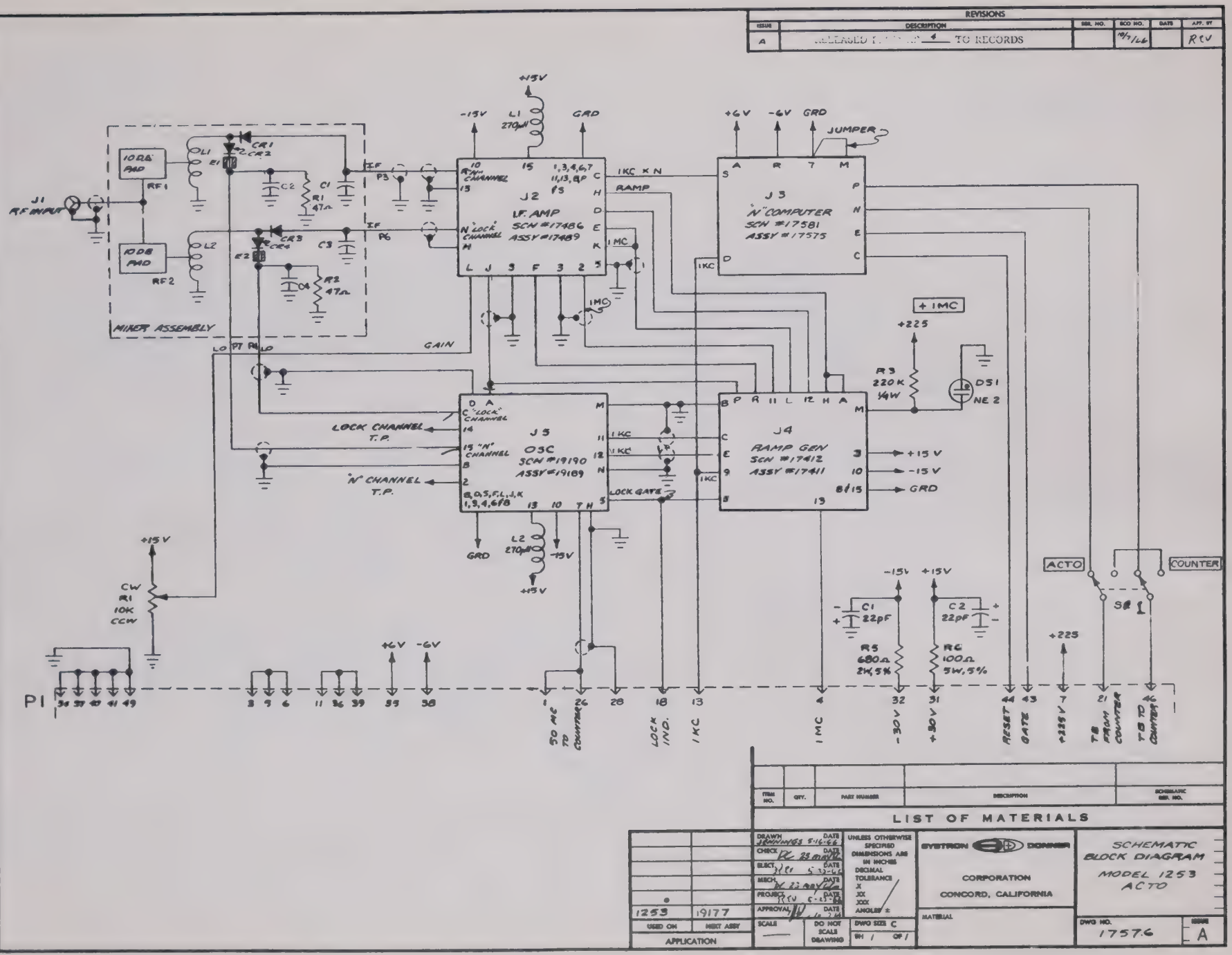
be generated in the two collector circuits. As a result, there would be no net current flow in the primary of T1. The presence of the one kilohertz signal on the base of Q1 creates an imbalance that causes a signal to flow in the collector circuit of one transistor during one half-cycle of the one kilohertz signal, and in the other collector circuit during the other half-cycle.

If the signal at either collector could be viewed without interference, it would appear as half-wave modulation envelopes containing the high frequency signal. The frequency being modulated is either 33 or 99 GHz. The two signals are added in the primary of T1.

The second transistor pair, Q3 and Q4, operate in a similar manner. It must be remembered, however, that the RF and modulating inputs bear the relationship to the Q1-Q2 inputs discussed earlier. The one kilohertz signal at the base of Q3 lags by ninety degrees the modulating signal to Q1; and the oscillator output at the Q3-Q4 emitters effectively leads the RF to Q1-Q2 by ninety degrees.

The signal at the primary of T1 represents the vectorial addition of the outputs of the transistor pairs. While the actual signals are difficult to diagram, Figure 4-8 depicts the principle involved using square waves. A five kilohertz input signal is shown being "rotated" by a one kilohertz modulating signal. The diagram accurately delineates the time/phase relationships and vector addition involved. The frequency shift in the output can be verified as follows: Count the number of times the input signal passes through a given point in a given direction during one cycle of the modulating signal (5). Now count number of times the output signal passes through the same point (4). If the modulating signal is shifted ahead 90°, the frequency shift will be additive. Any non-linearity in either the incoming or modulating signal will result in some frequency modulation being present on the output. This also will not affect the subsequent circuits.

The single-sideband output amplifier consists of two stages of tuned amplification, Q15 and Q16. The amplifier produces a 12 milliwatt output to the harmonic generator in the N channel mixer. A 47 ohm resistor, shown on the schematic block diagram, terminates the amplifier-mixer coax. The isolated test point on Pin 14 of J5 is provided for tuning the generator and amplifier.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CR2
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CR4
E1
E2
C1
C2
C3
C4
R1 47Ω
R2 47Ω
IF
P3
P6
J2
I.F. AMP
SCH #17486
ASSY #17489
"N" CHANNEL
"N" LOCK CHANNEL
J3
"N" COMPUTER
SCH #17581
ASSY #17575
JUMPER
+6V
-6V
GRD
-15V
+15V
1KC
1MC
RAMP
GAIN
LO
PT
J5
OSC
SCH #19190
ASSY #19189
LOCK CHANNEL T.P.
"N" CHANNEL T.P.
J4
RAMP GEN
SCH #17412
ASSY #17411
+1MC
+225
R3 220K 1/4W
DS1 NE 2
+15 V
-15 V
GRD
LOCK GATE
L2 270μH
CW R1 10K CCW
C1 22pF
C2 22pF
R5 680Ω 2W, 5%
R6 100Ω 5W, 5%
ACTO
COUNTER
SR 1
P1
TO MC TO COUNTER
LOCK IND.
1KC
1MC
-30 V
+30 V
RESET
GATE
+225 V
TO FROM COUNTER
TO TO COUNTER
LIST OF MATERIALS
ITEM NO.
QTY.
PART NUMBER
DESCRIPTION
SCHEMATIC REF. NO.
DRAWN J. RUNNELS 5-16-66
CHECK R. DONNER 5-23-66
ELECT. 5-23-66
MECH. R. DONNER 5-23-66
PROJECT. 5-23-66
APPROVAL 5-24-66
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±
SCALE
DO NOT SCALE DRAWING
DWG SIZE C
SH 1 OF 1
1253
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19177
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APPLICATION
SYSTRON DONNER
CORPORATION
CONCORD, CALIFORNIA
MATERIAL
SCHEMATIC BLOCK DIAGRAM
MODEL 1253
ACTO
DWG NO.
1757-6
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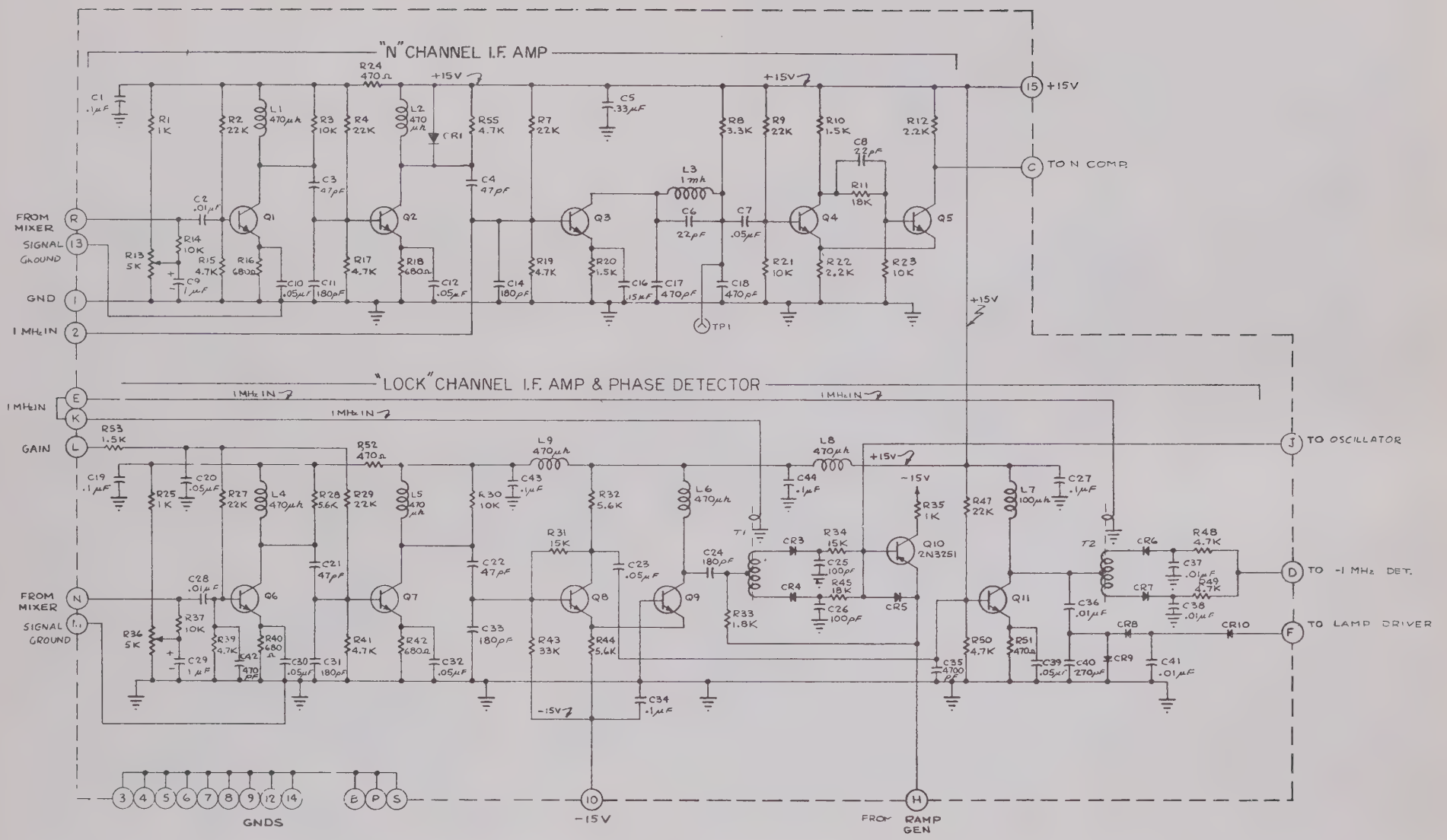


NOTE:
1. UNLESS NOTED—
ALL RESISTORS ARE 5%, ¼W
ALL TRANSISTORS ARE 2N706
ALL DIODES ARE CD6262

MODEL 1253 IF AMPLIFIER SCHEMATIC

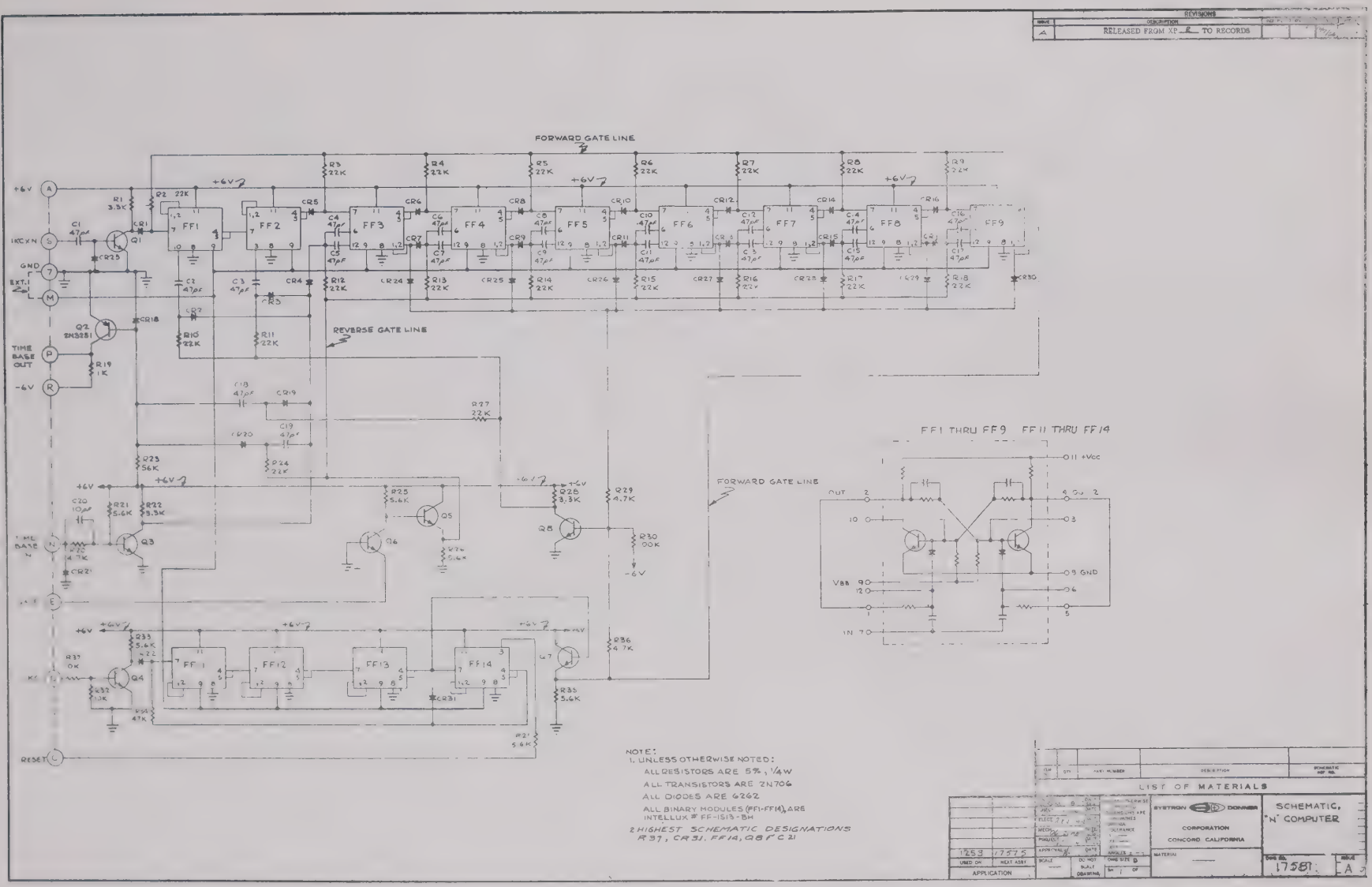
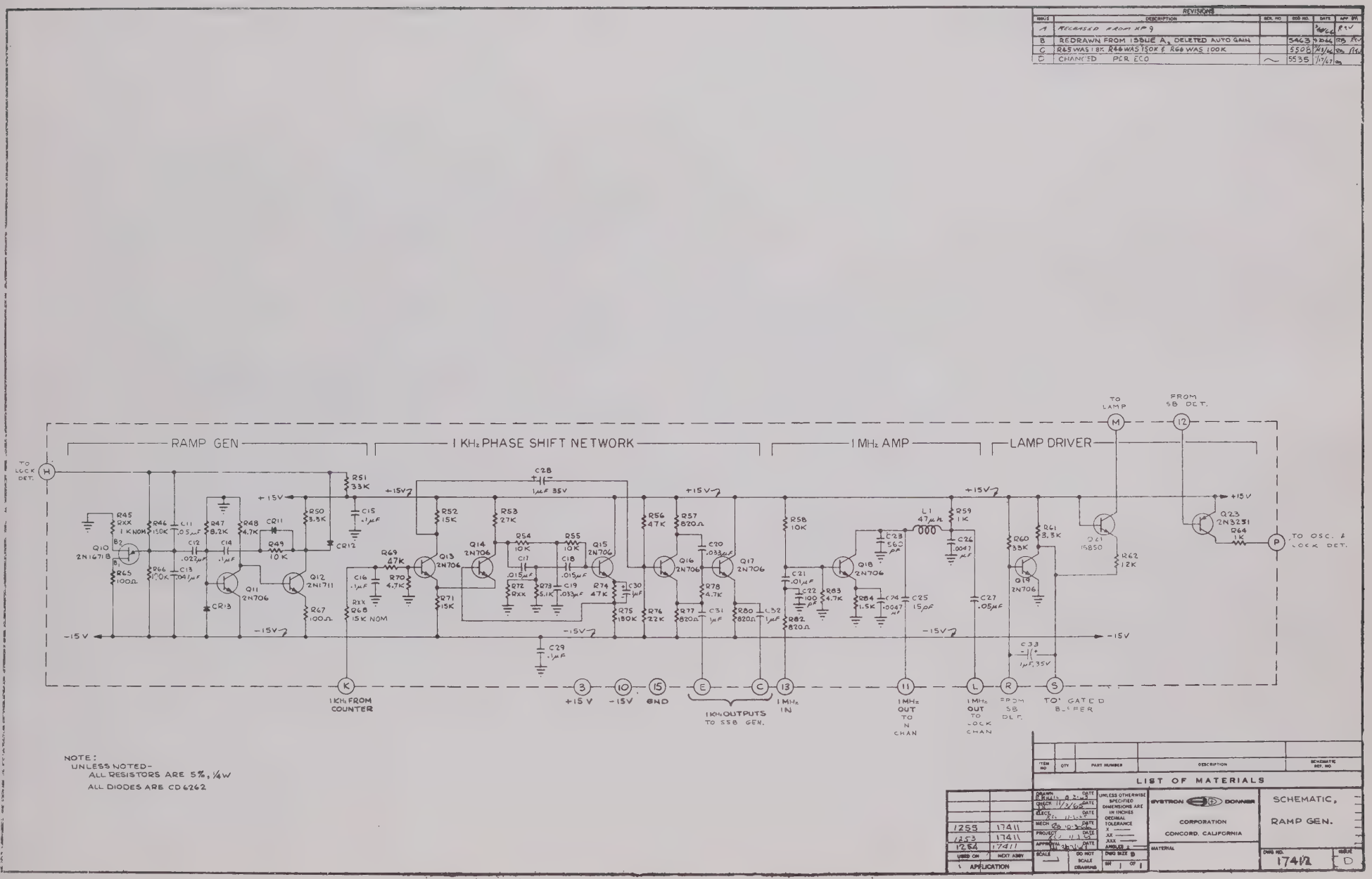


FIGURE 4-9 N COMPUTER SCHEMATIC


REVISIONS
ISSUE | DESCRIPTION | SER. NO | ECO NO. | DATE | APP BY
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B | REDRAWN FROM ISSUE A, DELETED AUTO GAIN | | 5463 | 4/26/66 | RW
C | R45 WAS 18K, R66 WAS 150K & R68 WAS 100K | | 5508 | 12/1/66 | RW
D | CHANGED PER ECO | ~ | 5535 | 1/17/67 |
RAMP GEN
1 KH₂ PHASE SHIFT NETWORK
1 MH₂ AMP
LAMP DRIVER
TO LOCK DET.
TO LAMP
FROM SB DET.
TO OSC. & LOCK DET.
+15V
-15V
1 KH₂ FROM COUNTER
+15 V
-15 V
END
1 KH₂ OUTPUTS TO SSB GEN.
1 MH₂ IN
1 MH₂ OUT TO N CHAN
1 MH₂ OUT TO LOCK CHAN
EPDM SB DET.
TO GATED BUFFER
NOTE:
UNLESS NOTED-
ALL RESISTORS ARE 5%, ¼W
ALL DIODES ARE CD 6262
LIST OF MATERIALS
ITEM NO | QTY | PART NUMBER | DESCRIPTION | SCHEMATIC REF. NO
SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
SCHEMATIC, RAMP GEN.
DWG NO. 17412
ISSUE D
1255 17411
1253 17411
1264 17411
USED ON | NEXT ASSY
APPLICATION

FIGURE 4-10 RAMP GENERATOR SCHEMATIC

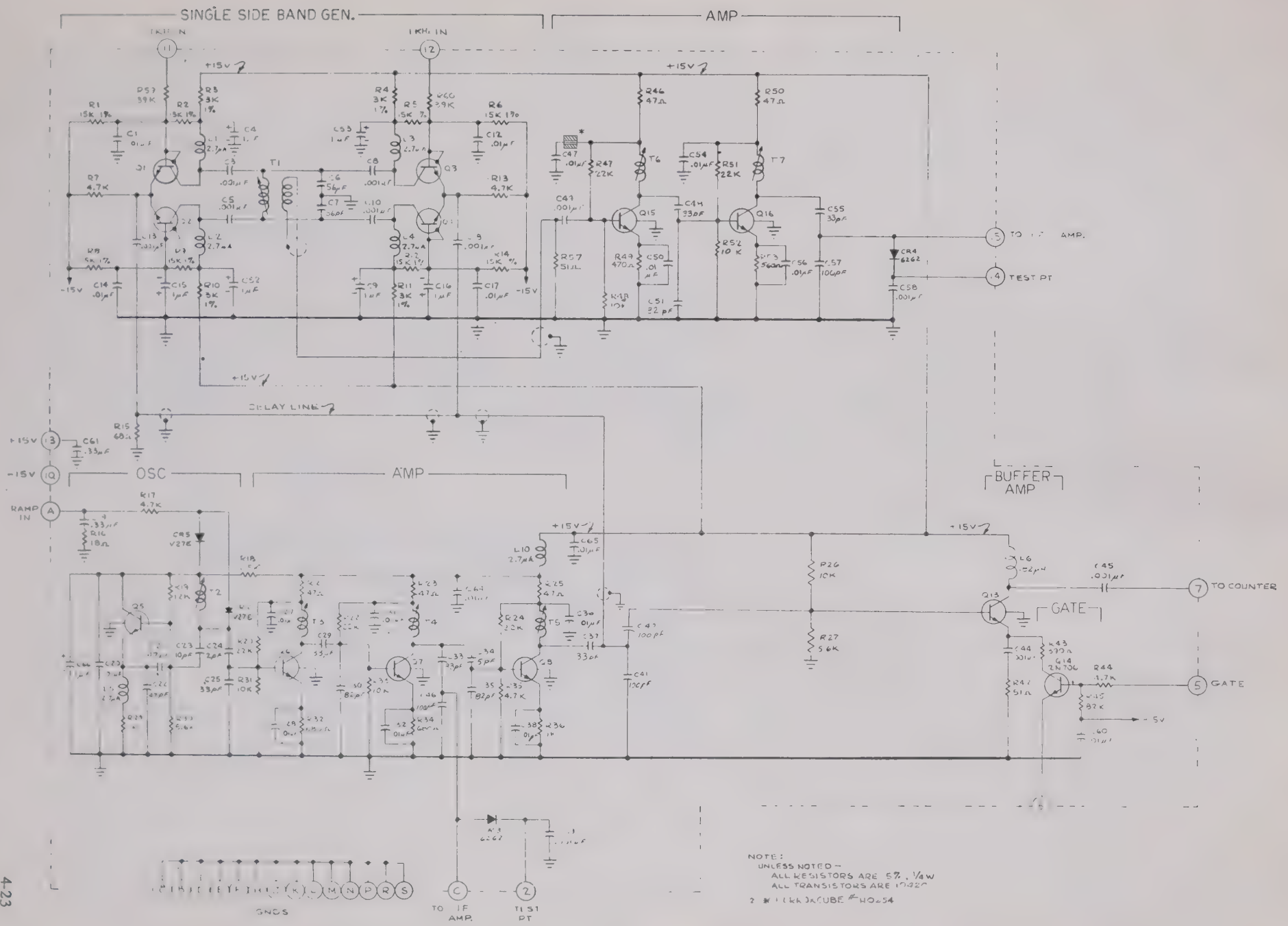
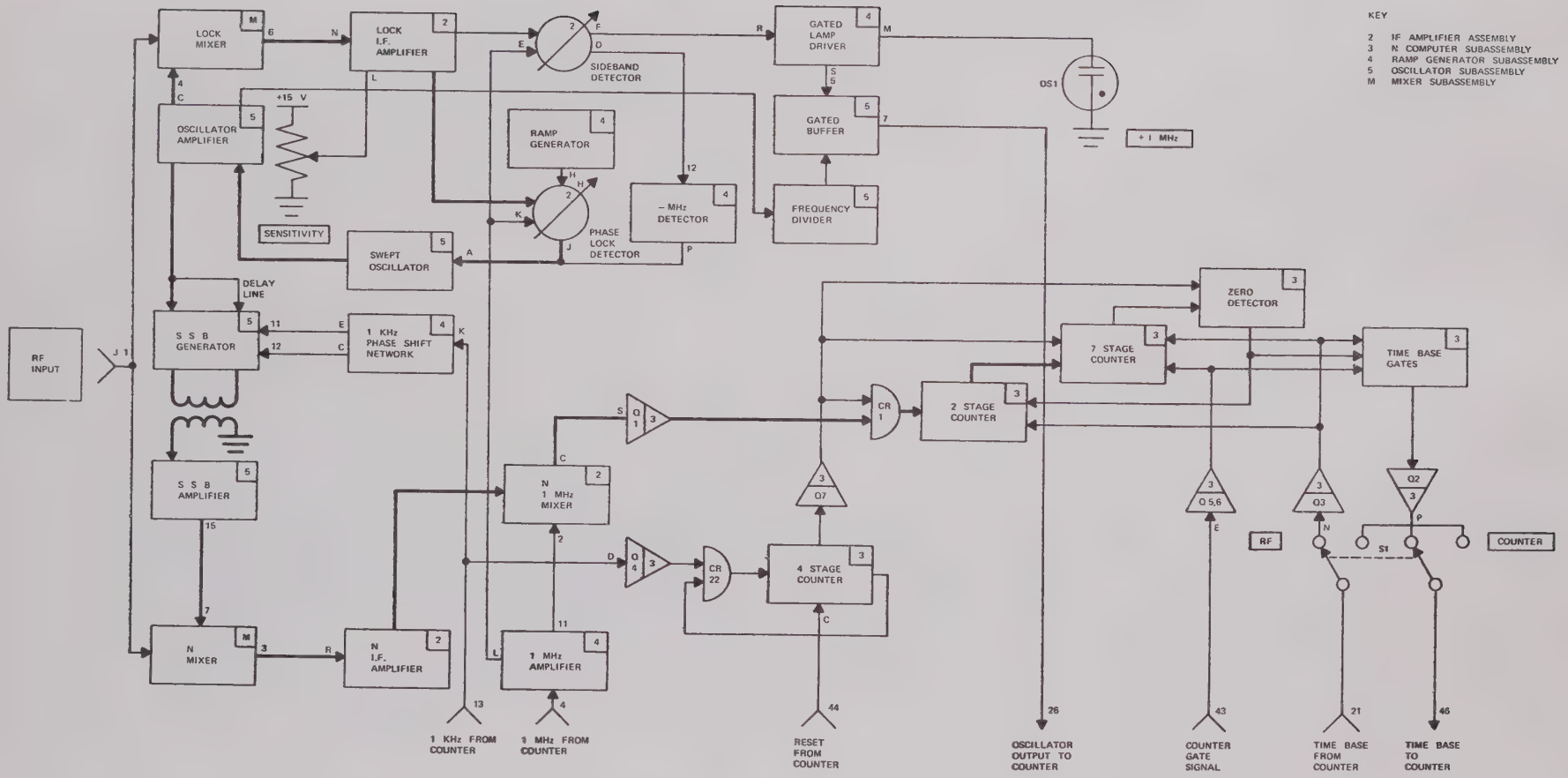


FIGURE 4-11 OSCILLATOR SCHEMATIC


KEY
2 IF AMPLIFIER ASSEMBLY
3 N COMPUTER SUBASSEMBLY
4 RAMP GENERATOR SUBASSEMBLY
5 OSCILLATOR SUBASSEMBLY
M MIXER SUBASSEMBLY
LOCK MIXER
LOCK I.F. AMPLIFIER
SIDEBAND DETECTOR
GATED LAMP DRIVER
OS1
+1 MHz
OSCILLATOR AMPLIFIER
+15 V
RAMP GENERATOR
GATED BUFFER
SENSITIVITY
PHASE LOCK DETECTOR
– MHz DETECTOR
FREQUENCY DIVIDER
SWEPT OSCILLATOR
DELAY LINE
ZERO DETECTOR
7 STAGE COUNTER
TIME BASE GATES
RF INPUT
J 1
S S B GENERATOR
1 KHz PHASE SHIFT NETWORK
2 STAGE COUNTER
S S B AMPLIFIER
N 1 MHz MIXER
4 STAGE COUNTER
N MIXER
N I.F. AMPLIFIER
1 MHz AMPLIFIER
1 KHz FROM COUNTER
3 MHz FROM COUNTER
RESET FROM COUNTER
OSCILLATOR OUTPUT TO COUNTER
COUNTER GATE SIGNAL
TIME BASE FROM COUNTER
TIME BASE TO COUNTER
RF
COUNTER
S1

NOTE

The following test, troubleshooting and alignment procedures should be performed only by competent technicians using proper tools and test equipment. Operating criteria and construction techniques preclude maintenance of this equipment by unskilled personnel.

5.1 GENERAL INFORMATION

The ACTO Plug-ins require no routine maintenance. As long as the unit is operating properly, alignment, disassembly or preventative maintenance should not be attempted. The basic operational check (see Section 5.2) is designed as an over-all test of ACTO operation, and serves as a "jumping-off" point for maintenance and alignment procedures.

5.1.1 TROUBLESHOOTING AND ALIGNMENT

The following test and troubleshooting procedures are designed to isolate malfunctions to blocks of circuitry corresponding approximately to the blocks on the Functional Block Diagram, Figure 5-3. The procedures should only be resorted to after all possibility of operator error or counter malfunction has been eliminated. In general, alignment procedures should only be used after replacement of components in a circuit affecting alignment.

The schematic diagrams are located after the text in this chapter. Adjacent to each subassembly schematic is a picture of the subassembly with callouts indicating test points, adjustments, and major components. Component location detail drawings are included with the parts lists at the back of the manual.

5.1.2 PHYSICAL DESCRIPTION AND DISASSEMBLY

Figure 5-1 shows, in simplified form, the exterior of an assembled ACTO, and the locations of screws involved in subassembly removal. In the case of screws 1, 2, and 3, similar screws exist on the opposite (unseen) side of the unit. Removal of the bottom shield plate is accomplished by loosening screws 4 and 5, and either 1 or the unseen screw opposite it. (The screws are not threaded into this plate. Consequently, complete removal of the screws is not necessary.)

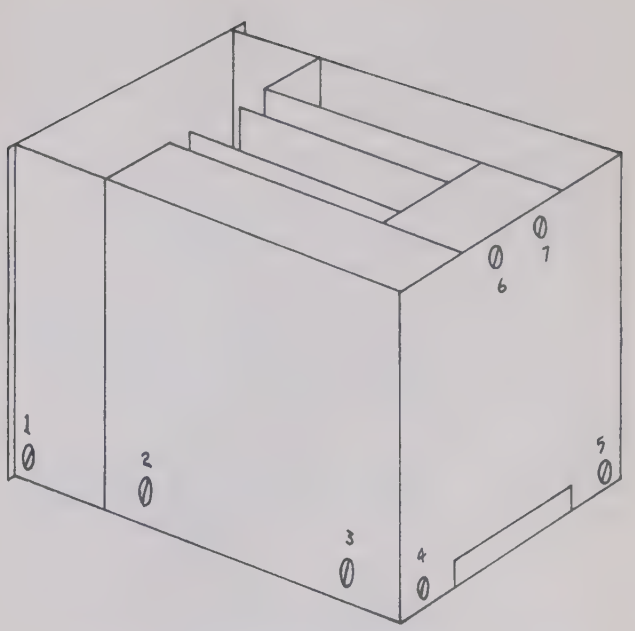


FIGURE 5-1 DISASSEMBLY SCREW LOCATION

Removal of the two center - mounted subassemblies (N Computer and Ramp Generator) is accomplished by loosening screws 6 and 7. This permits removal of the subassembly hold-down plate. The IF Amplifier subassembly is held in place by screws 2 and 3. It should be noted that all adjustments on this and the Oscillator subassembly are accessible without removing the subassemblies from the ACTO. The Oscillator subassembly is held in place by the unseen screws opposite 2 and 3.

The type of construction used on the Oscillator and IF Amplifier subassemblies requires that special care be exercised during repair of these boards. The component side of these boards is completely plated and etched only for a few signal leads. Since this plated surface is at ground potential, care must be taken that no unwanted solder "bridges" are formed during component replacement. When replacing components near a shield, care should be taken that leads not at ground potential do not come in contact with the shield.

5.1.3 RECOMMENDED TEST EQUIPMENT AND SET-UP

Listed below are test instruments required to troubleshoot and align the ACTO's. The same instruments and set - up are used for

both troubleshooting and aligning. This makes it easy to advance from one procedure to the next. Although particular instruments are specified below, any instrument with equivalent specifications may be substituted in every item except a.

a. Systron-Donner Counter Model 1017, 1018, 1037 or 1038 (ACTO's with option W may be checked out in a Hewlett-Packard Model 5245L or 5246L, however, no set - up procedures are given below for these counters.)

b. Table 5-1 lists signal generators that can be used for testing the ACTO's. In general, substitute generators should produce a signal between 100 mv rms and 500 mv rms (-7 dbm to +7 dbm) over the entire frequency range of the ACTO under test.

TABLE 5-1

1253	1254	1255
H-P 608	H-P 8616	H-P 620
612	618	626
8614	620	
8616		

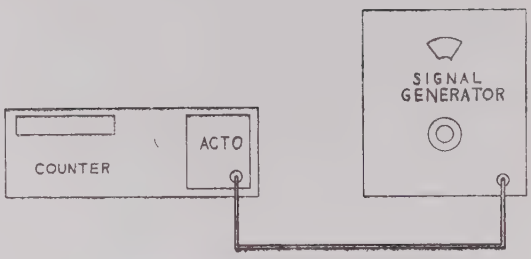
All generators shown are Hewlett - Packard

c. Tektronix Model 581 Oscilloscope with a Type 82 Dual-Trace Plug-in and x 10 probe. A substitute scope should be capable of dis - playing frequencies up to 100 MHz.

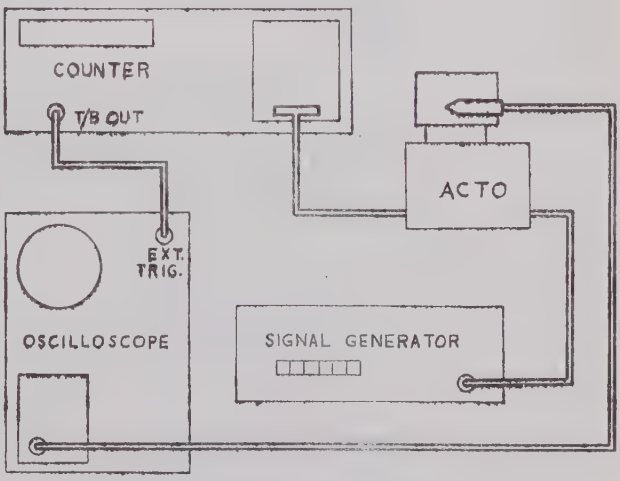
d. Simpson Model 260 Volt- Ohm - Milliammeter (20Kn/V).

e. Printed circuit board extender, Systron-Donner part number 11334.

f. Plug-in extender cable as per Figure 5-10.



Figures 5-2a and 5-2b are block diagrams of test set-ups. It should be noted that for some tests, the ACTO need not be placed on an extender cable.



NOTE

The most effective use may be made of the following procedures by starting at Section 5.2. Alignment must be accomplished in the sequence given, as earlier steps affect those that follow.

5.2 BASIC OPERATIONAL CHECK

The basic operational check serves as the ACTO Acceptance Test. In this capacity, it should be performed as soon as practicable after receipt of the instrument. Failure of any instrument to pass its acceptance tests should be brought to the immediate attention

of the nearest Systron-Donner representative. In its capacity as an overall test of system operation, the basic operational check can be used to define actual problem areas.

5.2.1 TEST SET - UP

The basic operational check is performed using the set-up shown in Figure 5-2a. Use and settings for counter controls not listed below can be found in Chapter 3 of the appropriate counter manual. Controls on the counter and ACTO should be set up as follows:

On the counter front panel, set the:

a. POWER switch to ON

b. TIME BASE switch to "10^{-3}"

c. FUNCTION switch to RATE

d. DISPLAY control to max.

e. RANGE switch to HET

f. LEVEL control to mid-range

On the ACTO, set the:

g. INPUT switch to RF

h. SENSITIVITY control to minimum sensitivity (MAX CCW)

Set up the signal generator as outlined in each individual procedure below. The signal generator should be capable of generating frequencies over the full specified range of the ACTO under test.

5.2.2 SENSITIVITY CHECK

a. Set the signal generator freq - uency to the lowest frequency the ACTO will measure (i.e., 300 MHz for the Model 1253, 2. 96 GHz for the Model 1254, or 8.2 GHz for the Model 1255).

b. Set the signal generator output signal level to 100 mv rms (-7 dbm).

c. Rotate the ACTO SENSITIVITY control clockwise until the "+1 MC" light is ON.

d. Verify that the counter readout is accurate and stable. (The light on the ACTO indicates that 1 MHz must be added to the readout.)

e. Repeat frequency measurements at 500 MHz intervals until the maximum ACTO frequency is reached.

5.2.3 OVERLOAD CHECK

a. Set the signal generator to the lowest frequency the ACTO will measure.

b. Set the signal generator output signal level to 500 mv rms (+7 dbm).

c. Rotate the ACTO SENSITIVITY control clockwise until the "+1 MC" light is ON.

d. Verify that the counter readout is accurate and stable.

e. Repeat frequency measurements at 500 MHz intervals until the maximum ACTO frequency is reached.

5.3 GENERAL TEST PROCEDURE

The general test procedure is arranged in three general phases: In-counter operational tests, input signal verification, and ACTO internal signal tracing. Actual removal of subassemblies is postponed until late in the second phase. Unnecessary removal of sub-assemblies or replacement of components is discouraged.

Many circuits in the ACTO interact, making repair and alignment a qualitative process. The test procedures are arranged as a series of notes suggesting sequential processes to be followed in the isolation of a malfunction. In general, the troubleshooting process is or-ganized around the functional block diagram (Figure 5-3). Isolation of failed components is left up to the technician. No description of a particular symptom and its cause is meant to be exclusive of other failures that may produce the same indication.

5.3.1 IN-COUNTER OPERATIONAL TESTS

Set up the counter and ACTO as described for the basic operational check. Inject some frequency near the middle of the range of the ACTO under test and attempt to lock on. Then proceed with the following test.

If the "+MC" light does not come on and the readout is incorrect or unstable, a problem probably exists in the lock channel or its supporting circuitry. In this case, Test b. below will probably be inconclusive, since the oscillator may still be sweeping. If the light does come on and the readout is inaccurate, tests a. and b. will help determine the general problem area.

a. Independently determine the approximate value of N. (To compute N, divide the input frequency by the ACTO swept oscillator center frequency.) Place the counter FUNCTION switch in the TEST position. The counter readout should be N x 10 MHz or 2N x 10 MHz in the 1254 and 1255.

b. Place the counter FUNCTION switch in the RATE position. Move the ACTO INPUT switch to the COUNTER position. The counter readout should be the oscillator frequency in the Model 1253 or half the oscillator frequency in the 1254 or 1255.

Several possible combinations of basic symptoms (i.e., correct or incorrect readout, indication of lock, harmonic number, or oscillator output) have now been developed. Table 5-2 summarizes the possible problem areas.

TABLE 5-2

GENERAL TROUBLESHOOTING GUIDE

SYMPTOMS	POSSIBLE TROUBLE AREA
Lock light off, readout incorrect, oscillator incorrect, N correct	Lock loop
Lock light on, readout incorrect, oscillator correct, N incorrect	N channel
Lock light off, readout correct, oscillator correct, N correct	Gated lamp driver, + 225 power supply, Neon bulb
Lock light on, readout incorrect, oscillator incorrect, N correct	Oscillator output link to counter
Lock light off, readout incorrect, oscillator incorrect, N incorrect	± 15 supply, 1 MHz input

5.3.2 INPUT SIGNAL VERIFICATION

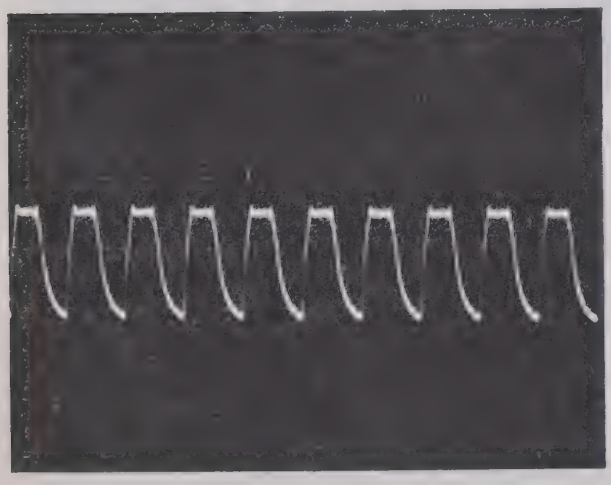
To allow access to the input signals from the counter, shut off the counter and remove the ACTO. Remove the bottom shield plate, following the instructions in Subsection 5.1.2. Invert the ACTO so that the subassembly connectors are accessible and use the test set-up diagrammed in Figure 5-2b.

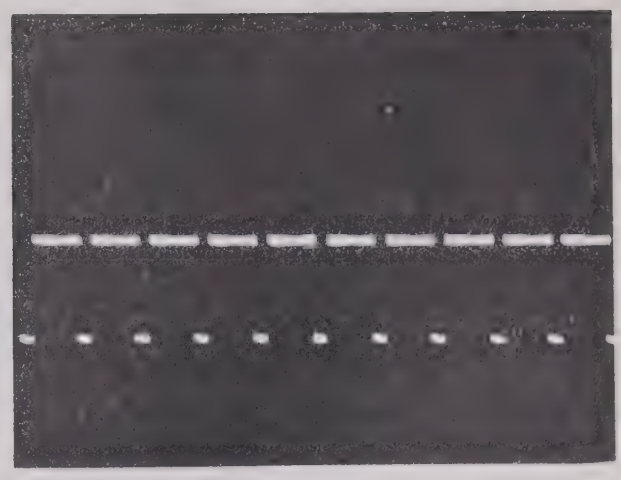
Before re-energizing the counter, inspect the visible components. Re-energize the counter and attempt to lock on the ACTO. Use the appropriate schematic block and chassis layout diagrams to locate the access points for the following tests.

a. Check the ±30 volts. These voltages are used to develop the ±15 volts used on every subassembly except the N computer.

b. Check the ±6 volts. These supplies are used only on the N computer.

c. Check the +225 volts. This voltage is used only to light the "+1 MC" indicator. The +225V supply is accessible on the terminal strip on the rear of the front panel.





e. Check the 1 KHz signal. The signal should look like Figure 5-5. This is the input to the one kilohertz phase shift network on the Ramp Generator subassembly.

f. Check the time base, GATE, and RESET inputs. The rate of recurrence of the signals is controlled by the settings of counter front panel controls.

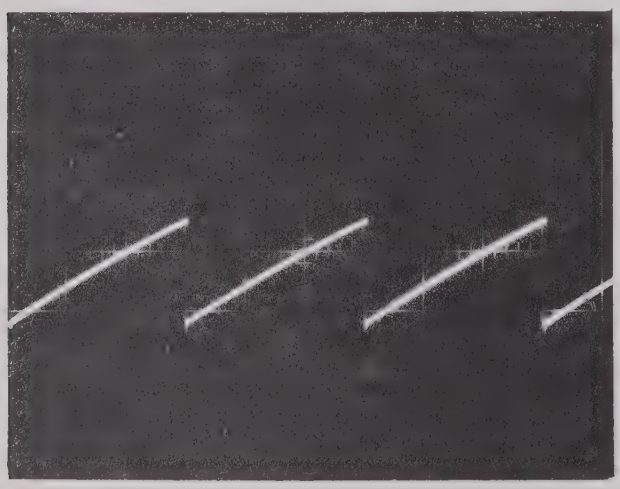
Watch for unusual loading effects on these input signals.

5.4 ACTO INTERNAL SIGNAL TRACING

The functional block diagram, Figure 5-3, is a good aid to understanding the operating relationships being tested in this section. If all the voltages and signals from the counter appear to be normal, the next step is to check for the presence of signals generated in and processed by the ACTO. The logical sequence in which to perform the following tests is dictated by the symptoms already observed. For example, tests relating to the N channel need not be performed if it has already been determined that the N channel is operating properly.

The test set-up shown in Figure 5-2b is used for the following tests. In some cases, a subassembly must be placed on an extender board to allow observation of a signal. Instructions for removing the subassemblies are contained in Subsection 5.1.2. When a subassembly is removed, inspect it carefully for physical evidence of a malfunction. Do not remove the subassemblies unnecessarily.

For the following tests, set up the ACTO and counter as described for the basic operational check. Any variations from this set-up will be described as the tests proceed. When an input signal is called for, it should be within the range of the unit under test and above the minimum signal level (100 mv rms).

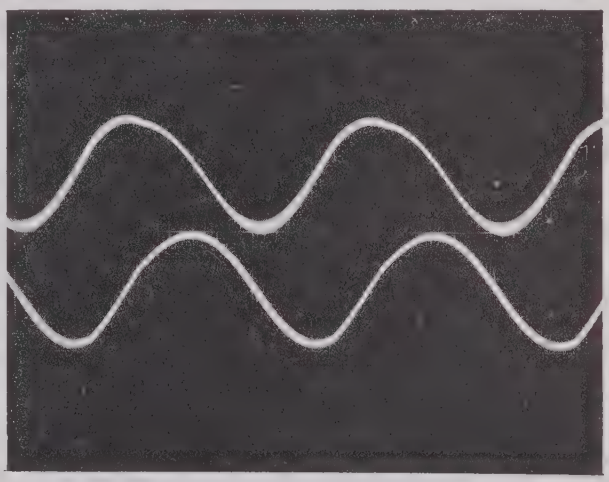


5.4.1 RAMP GENERATOR CHECK

The output of the ramp generator can be observed at Pins H or A of J3, if the ACTO is not locked on. Figure 5-6 shows the ramp. If rotating the ACTO sensitivity control clockwise causes the ramp to stop, this is a good indication that the lock channel "loop" is operating properly.

5.4.2 1 MHz AMPLIFIER CHECK

The one megahertz amplifier is one of the two functional elements common to both channels. (The other is the oscillator.) The two sinusoidal outputs of the amplifier may be observed at pins L and 11 of J4. Loss of the 1 MHz signal to either channel will prevent operation of that channel.



5.4.3 1 KHz PHASE SHIFT NETWORK CHECK

Failure of the one kilohertz phase shift network will affect only the N channel. Figure 5-7 shows the phase relationship between the two outputs from the network.

5.4.4 OSCILLATOR OUTPUT CHECK

Short to ground Pin A on J4. This halts the ramp so that the output of the oscillator may be observed. With the Oscillator subassembly on the extender board, the unamplified oscillator output can be observed at the base of Q6.

> CAUTION: The loading affect of the oscilloscope will alter the oscillator frequency.

The proper operation of subsequent stages of amplification can be verified by observing the bases of Q7 and Q8, and the input to the binary or buffer. The output to the lock channel is taken at Q7, and to the N channel at Q8.

The oscillator output to the counter passes through a flip-flop frequency divider in the Models 1254 and 1255. The operation of this flip-flop can be observed at the base of Q 13. When the ACTO is not locked on, the oscillator signal does not pass Q13. Operation of this gated buffer is discussed in Subsection 5.4.5.

CAUTION: When this test is completed, remove the ground from Pin A of J4.

5.4.5 LOCK CHANNEL OPERATION CHECK

If the ACTO does not lock on, the malfunction is probably in the "lock loop" as shown on the functional block diagram. Only those elements of the loop not previously checked are discussed here. It should be noted that the ACTO can lock on and still not provide an output to the counter if the oscillator output link fails. This circuitry is discussed in Subsection 5.4.4.

a. Operation of the IF amplifier can be observed by extending the IF Amplifier subassembly and checking the base of Q8.

b. Mixer operation can be checked by interchanging the two mixers. Instructions for replacing the mixer diodes are given in Subsection 5.5.

c. Operation of the phase lock detector can be observed at Pin J of J2. If the ACTO is not locked on, this point should exhibit the ramp (Figure 5-5). When the ACTO locks on, the ramp should stop.

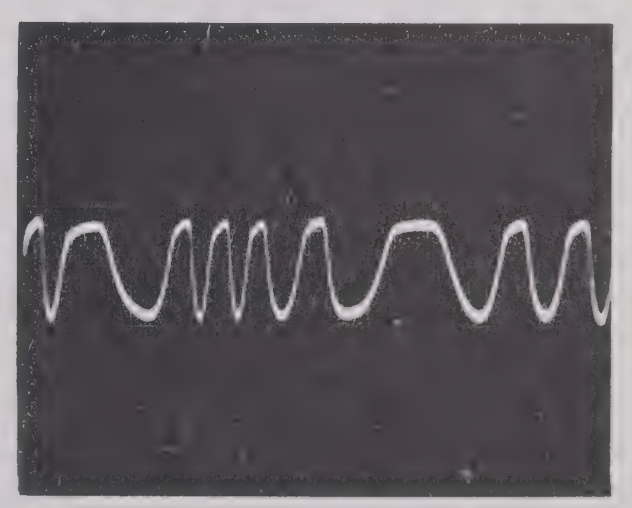
d. The sideband detector produces two outputs: A gate signal to the lamp driver at Pin F of J2, and an output to the 1 MHz detector at Pin D. The gate signal should be approximately +1 v at lock and -4 v when the ACTO is not locked on. The output at Pin D should be +0.5 v, biased at +15 v when locked.

e. Operation of the gate signal to the gated buffer can be observed at Pin 5 of J5. The signal should be near ground when the ACTO is not locked on, and approximately +10 v at lock.

5.4.6 N CHANNEL OPERATION CHECK

The N channel circuitry is arranged sequentially. Troubleshooting, therefore, is a matter of tracing the signal through the channel from block to block. The following is a list of sequential points at which the N channel signal and supporting signals may be observed:

a. With a VOM, check the voltage at Pin 14 on J5. It should be +0.75 v or more. If any signal tracing is done in the single-sideband amplifier, the ground lead must be located as close as possible to the point being observed.



b. Check TPI on the IF Amplifier subassembly. The signal should look approximately like Figure 5-8. This is the 1 KHz x N signal before it is shaped. The output of the shaper can be observed at Pin C of J2.

All of the following test points are on the N Computer subassembly. The subassembly must be placed on an extender board to allow access to the signals.

c. Observe the 4 ms forward gate signal at the base of Q7. This signal is developed by the third

stage of the four-stage counter. The drive signal for this counter is a 1 KHz signal, observable at the collector of Q7.

d. The drive signal to any counter stage is visible on Pin 7 of that stage. (See Fig. 4-5 for Pin location.)

e. The reverse gate signal can be observed on the emitter of Q5. The duration of this pulse is a function of the counter TIME - BASE switch and DISPLAY control settings.

f. The output of the zero detector is developed at the collector of Q8.

g. The counter time base signal should always be present at the collector of Q3. In the Models 1254 and 1255, every other time base pulse should be present at the junction of CR32 and CR33.

h. Groups of time base pulses should be present at the collector of Q2 when the ACTO is locked on.

5.5 ALIGNMENT PROCEDURES:

The following alignment procedures should be undertaken only by persons with a thorough knowledge of the principles on which the ACTO operates. The alignment should be considered a qualitative process aimed at producing the optimum in ACTO operation.

5.5.1 IF AMPLIFIER SUBASSEMBLY

Turn potentiometers R13 and R36 fully counter clockwise. This grounds the arm of the potentiometer and will normally produce the best operation.

5.5.2 OSCILLATOR SUBASSEMBLY

Tuning of the oscillator and single - sideband generator and their tuned amplifiers can be accomplished with the subassembly installed in the ACTO. All adjustments are accessible through the shield plate. The layout diagram opposite the oscillator schematic can be used to locate the various adjustments.

To tune the oscillator:

a. Use the test set-up diagrammed in Figure 5-2b.

b. Set up the counter and ACTO as described in Subsection 5.2.1.

c. Set the ACTO INPUT switch to COUNTER.

d. Short to ground Pins A and R on J4. (This stops the oscillator sweep and opens the gate to the counter.)

e. Tune T2 until the counter reads 31.5 - 32 MHz in the Model 1253 or 48.5 - 49 MHz in the Models 1254 and 1255. (This is only one-half the oscillator frequency in the latter two models.)

f. Remove the short from Pins A and R of J4.

g. Tune T3 and T4 for maximum voltage at Pin 2 of J5. This should be +0.75 volts or better.

h. Tune T5, T1, T6, and T7 for maximum voltage at Pin 14 of J5. This should be +0.75 volts or better. (The adjustments in steps e, g, and h interact.)

5.5.3 RAMP GENERATOR SUBASSEMBLY

There are two factory selected resistors on the Ramp Generator subassembly: R45 in the ramp generator and R72 in the one kilohertz filter. The following steps detail the selection process.

In the Model 1253:

a. Connect the vertical input of the oscilloscope to TP1 on the IF Amplifier subassembly.

b. Connect the horizontal input of the oscilloscope to Pin H on J4.

c. Inject a signal of 270 MHz and 100 mv. Rotate the SENSITIVITY control fully counter-clockwise.

d. Select a value for R45 that causes the oscilloscope to display two beats.

e. Inject a signal of 300 MHz and 100 mv and lock on with the ACTO.

f. Synchronize the oscilloscope with the counter time base. Set the counter TIME BASE switch to "10^{-3}" and the oscilloscope sweep speed to 200 us per cm.

g. Select a value of R72 that results in the least frequency modula - tion of the observed waveform.

Perform the same procedure in the Model 1254, except: In step c., change the frequency to 2.7 GHz, and in step e., change the frequency to 3 GHz.

Perform the same procedure in the Model 1255, except: In step c., substitute 7.6 GHz for the frequency and in step e., substitute 9 GHz.

5.6 MIXER DISASSEMBLY

Replacement of the mixer diodes in the Models 1254 and 1255 requires the disassembly of the mixer subassembly. Figure 5-9 is a cutaway view of a typical mixer. (In some later models, the mixer block is formed from a single piece of metal.) Disassembly of the mixer is a relatively simple operation Re - assembly is somewhat more critical and must be done with care to achieve optimum operation.

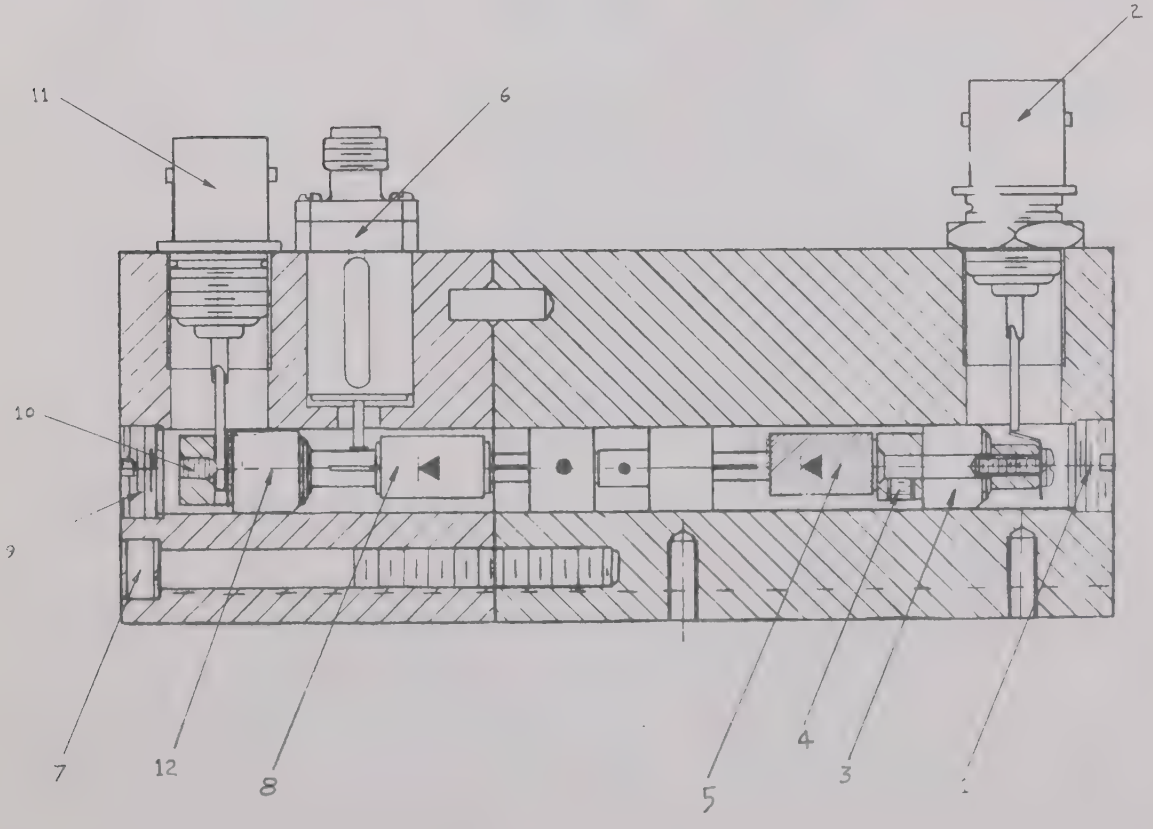


FIGURE 5-9 MIXER DISASSEMBLY DIAGRAM

a. Remove the malfunctioning mixer from the ACTO by removing the two screws that fasten the mixer to the body of the plug-in.

b. Disconnect the input and output cables, tagging the cables to prevent confusion at reassem - bly.

c. Refer to the diagram. To re - move the harmonic generator diode, item 5, first remove the end plug, item 1.

d. Remove the oscillator input connector, item 2.

e. Remove the slug assembly, item 3.

f. To remove the diode, loosen the set - screw, item 4. Remove and save the resistor film from the body of the diode. In later models, this film will not be present.

g. To remove the mixer diode, item 8, loosen the set screw holding the RF input connector, item 6, and remove the connector. Be careful not to lose the small square of tape on the end of the input probe.

h. In the models with a two -section mixer block, removing the screw, item 7, will allow access to the diode.

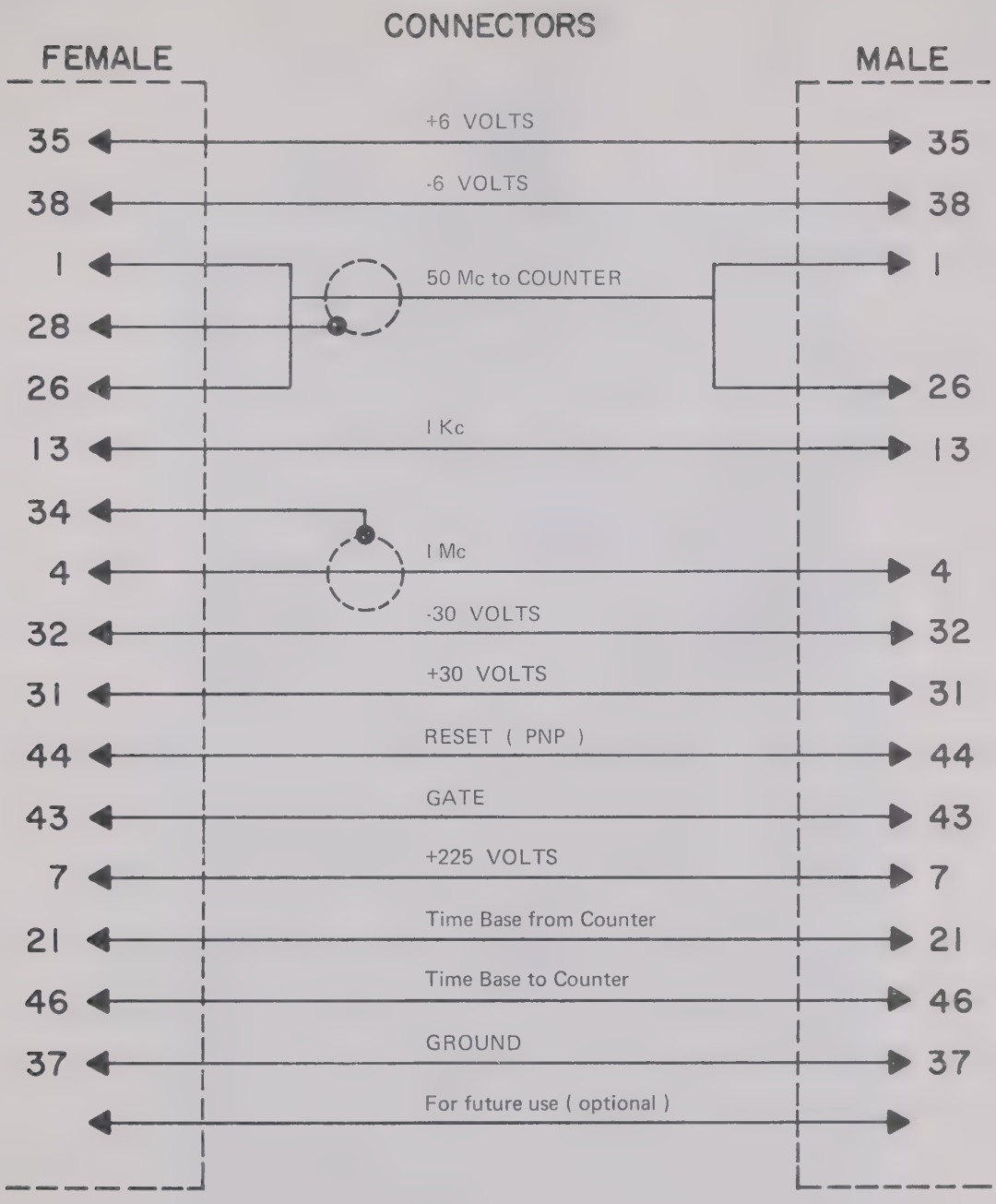
i. In units with a solid mixer block, remove the end plug, item 9.

j. Loosen the set screw, item 10, and unscrew the IF output con- nector, item 11.

k. Remove the slug assembly, item 12.

l. If the diode does not come out with the slug assembly, use a pair of tweezers to remove the diode.

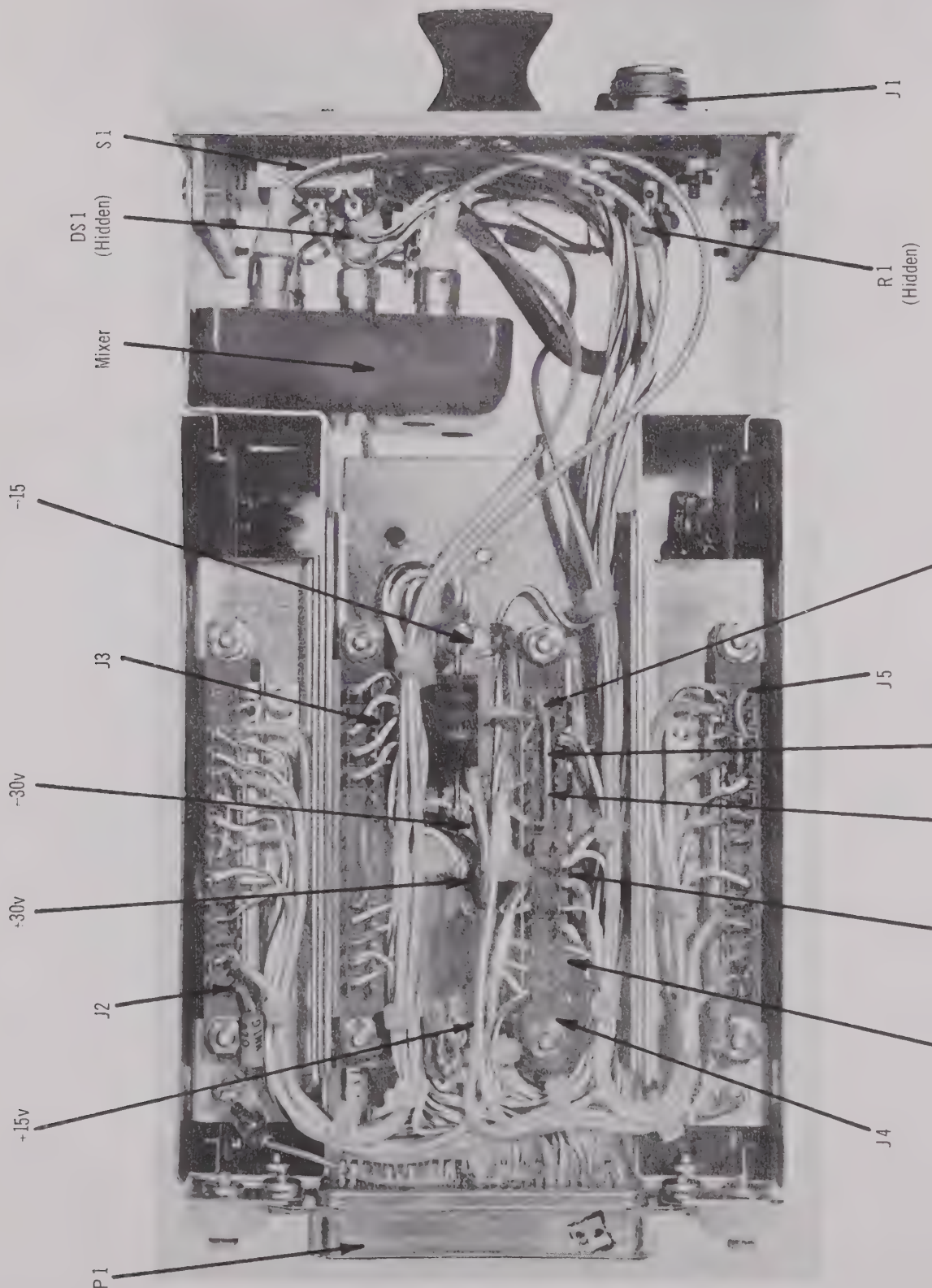
Re-assembly of the mixer is the reverse of the disassembly process. Care must be taken when reinserting the RF input connector, item 6, that the small square of tape is in place at its tip. This tape serves as a dielectric. The mixer will not operate with the RF input probe shorted to the diode. When reinserting the oscillator input connector, make sure that the probe firmly contacts the spring contact on the slug assembly. This contact can be observed with end plug, item 1, removed.



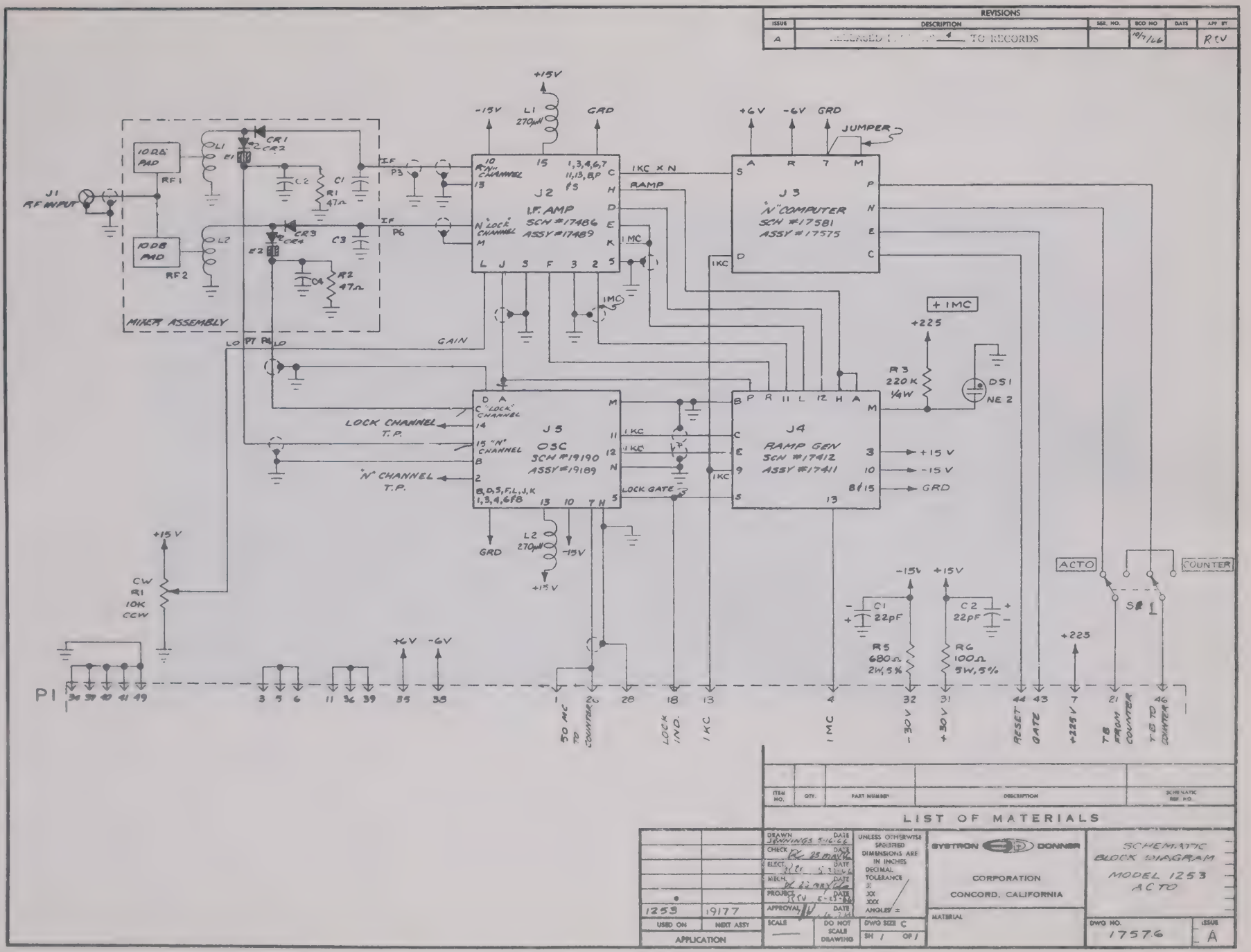
NOTES:

1. All wires number 22 teflon, except 1, 26, & 4 which are coax and 37 which is number 18 teflon
2. Male Connector is 50 pin, Amphenol Blue Ribbon, P/N 57-30500
3. Female connector is 50 pin, Amphenol Blue Ribbon, P/N 57-40500-2
4. All wire lengths should be approximatly 2 feet

Figure 5-10 Acto Extension Cable



MODEL 1253 CHASSIS LAYOUT

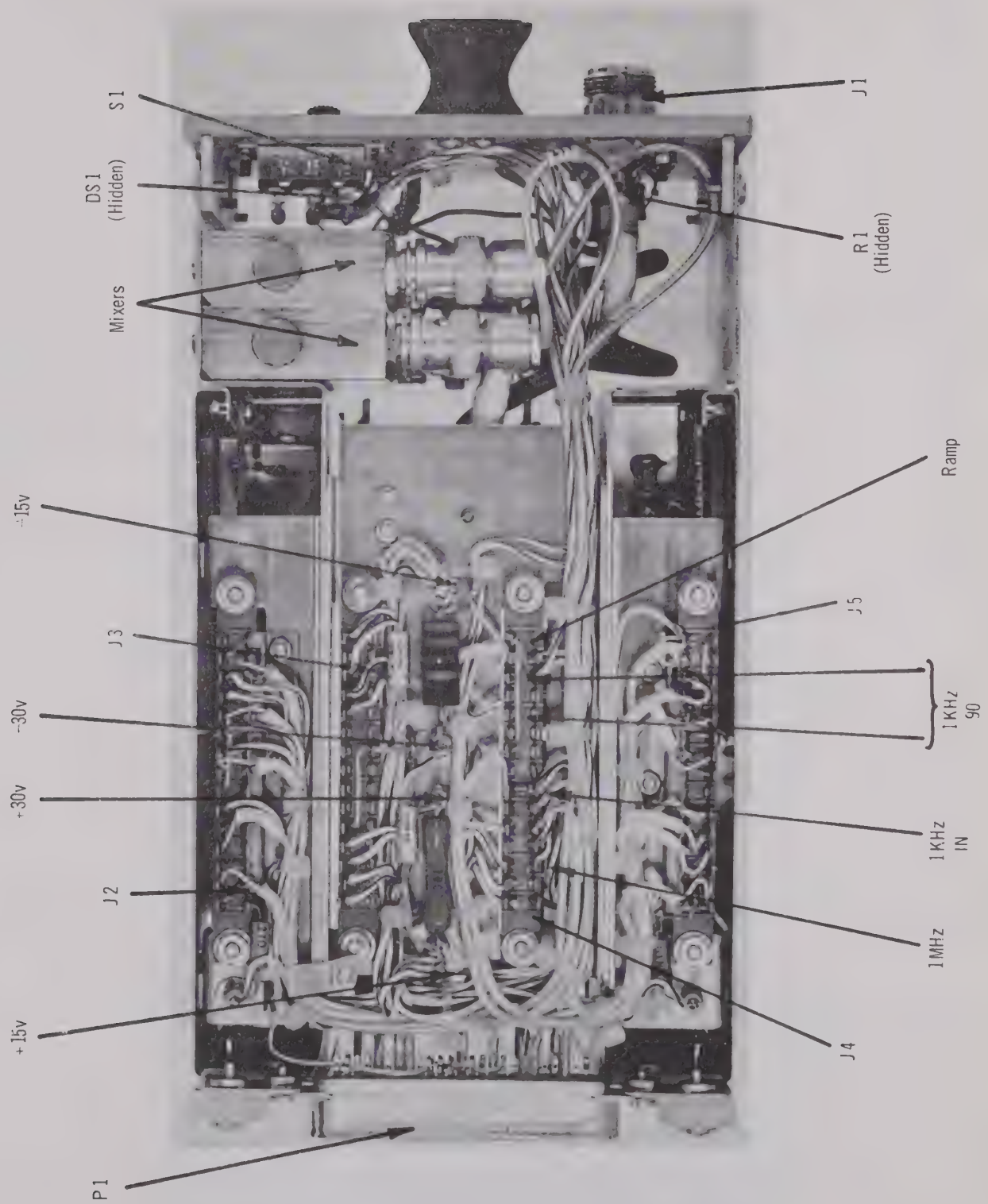


ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

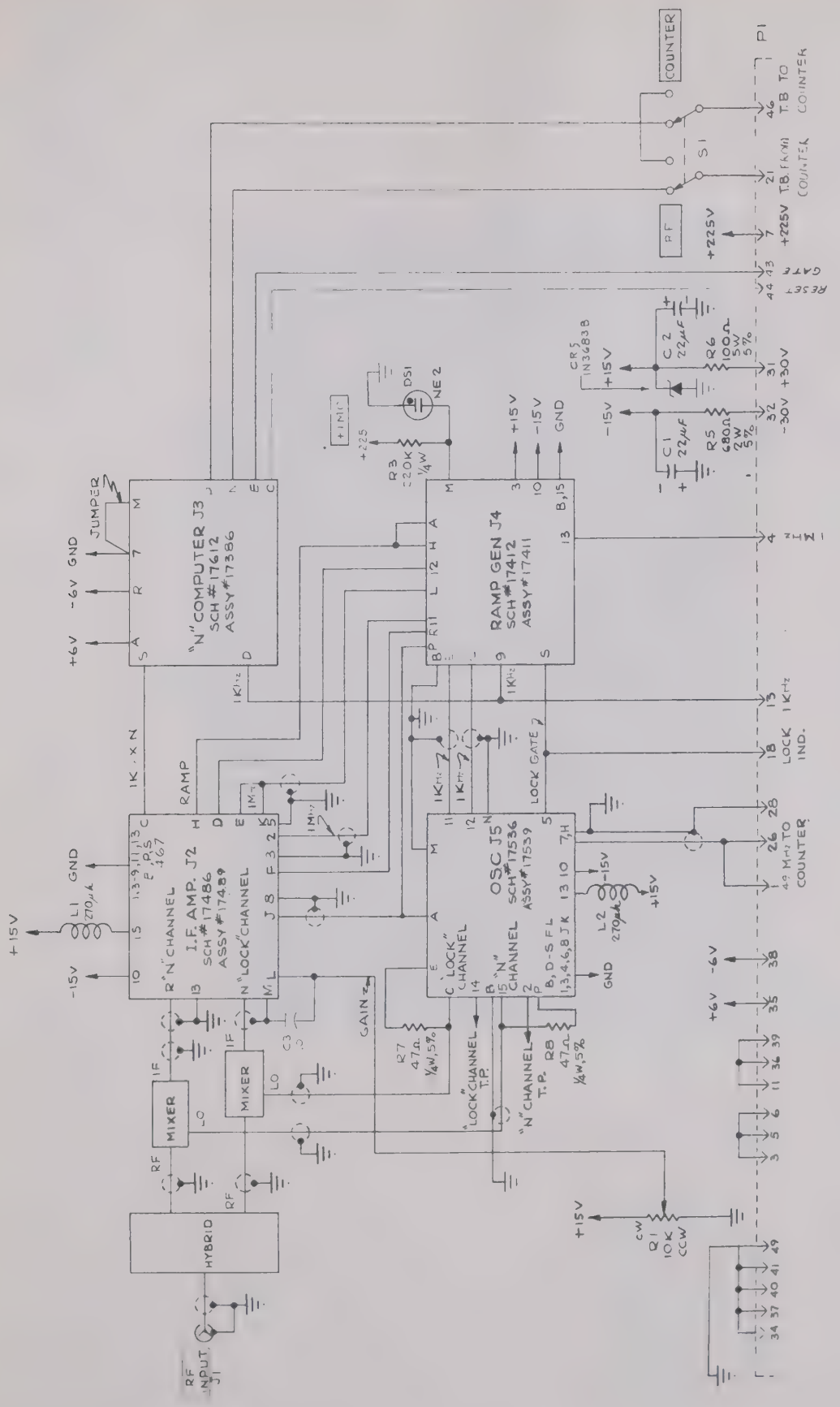
LIST OF MATERIALS

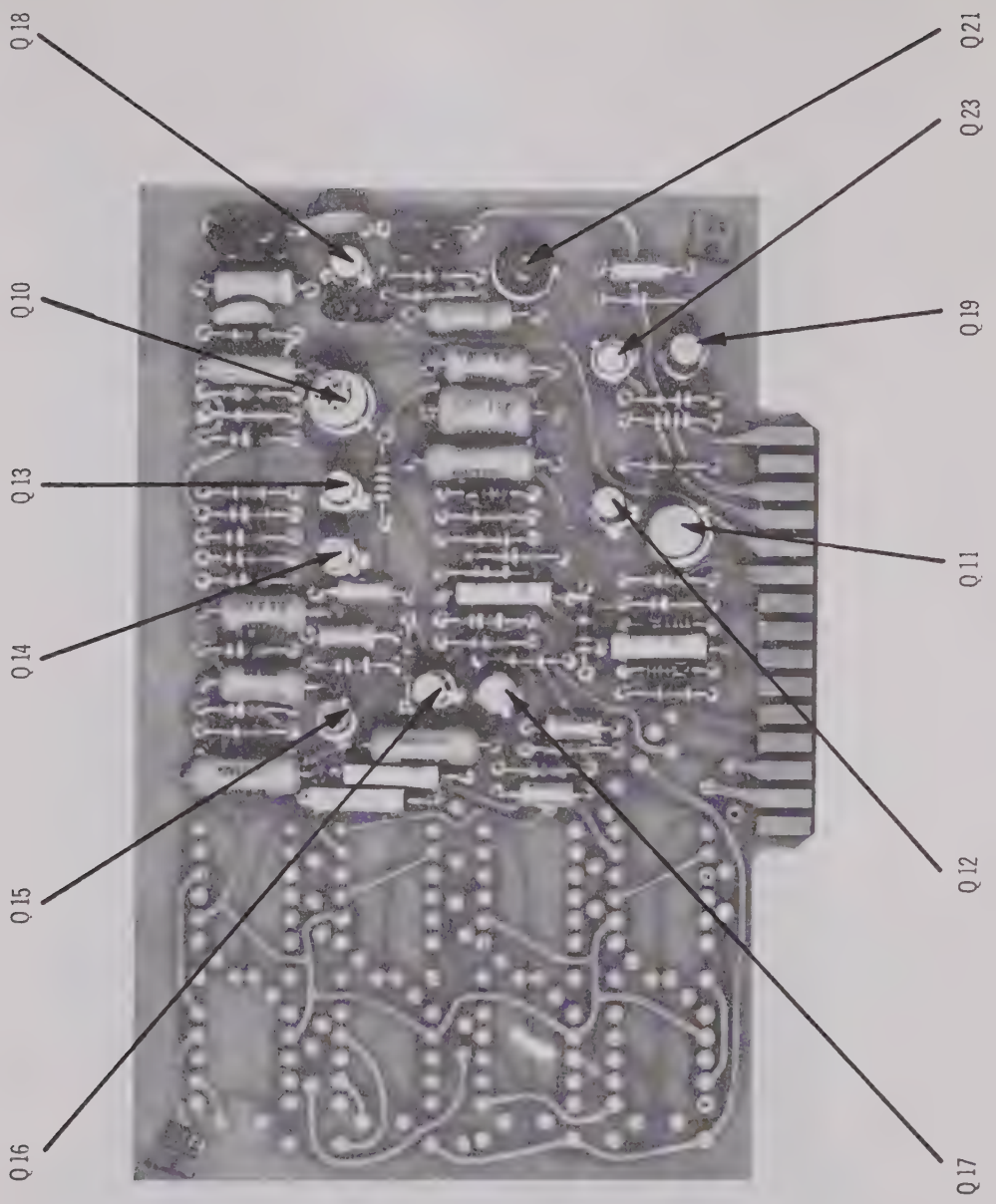
DRAWN	JENNINGS	5-16-66	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	SCHEMATIC BLOCK DIAGRAM MODEL 1253 ACTO
CHECK	RC 25 MAY 66	DATE			
ELECT.	RCV	5-31-66			
MECH.	RC 22 JUNE 66	DATE			
PROJECT	RCV	6-23-66			
APPROVAL		DATE			
SCALE		DO NOT SCALE DRAWING	DWG SIZE C SH 1 OF 1	MATERIAL	DWG NO. 17576 ISSUE A

1253	19177
USED ON	NEXT ASSY
APPLICATION	



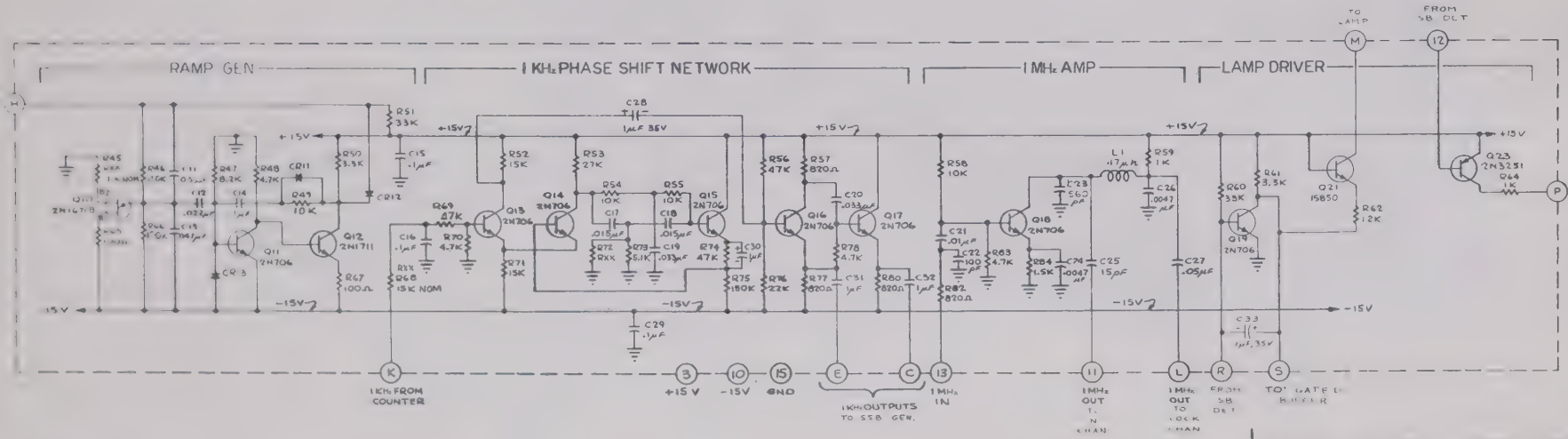
MODEL 1254 and 1255 CHASSIS LAYOUT


"N" COMPUTER J3
SCH #17612
ASSY #17386
RAMP GEN J4
SCH #17412
ASSY #17411
I.F. AMP. J2
SCH #17486
ASSY #17489
OSC J5
SCH #17536
ASSY #17539
"N" CHANNEL
"LOCK" CHANNEL
RAMP
LOCK GATE
JUMPER
+6V
-6V
GND
+15V
-15V
+225V
-30V
+30V
COUNTER
P1
S1
PF
DS1
NE2
CR5
1N3683B
C1
C2
R1
R2
R3
R5
R6
R7
R8
L1
L2
MIXER
HYBRID
RF INPUT J1
LOCK IND.
TO COUNTER
GAIN
CW
CCW



RAMP GENERATOR LAYOUT

REVISIONS					
ISSUE	DESCRIPTION	DESC. NO.	ECO NO.	DATE	APP. BY
A	RELEASED FROM NP 9			3/24/66	[illegible]
B	REDRAWN FROM ISSUE A, DELETED AUTO GAIN		5463	9/24/66	[illegible]
C	R45 WAS 1.8K R46 WAS 150K & R66 WAS 100K		5508	10/31/66	[illegible]
D	CHANGED PER ECO	~	5535	1/17/67	[illegible]



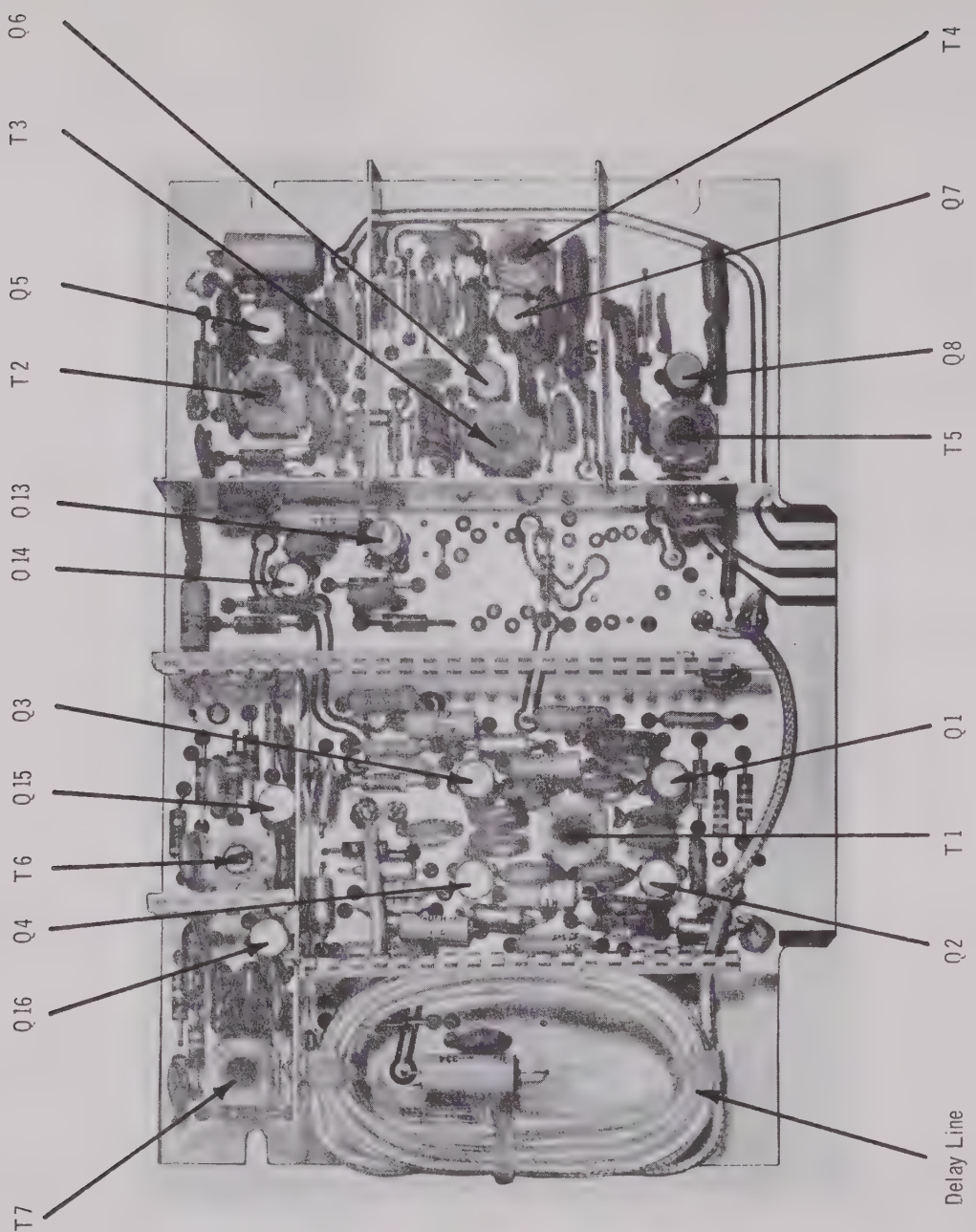
NOTE:
UNLESS NOTED -
ALL RESISTORS ARE 5%, ¼W
ALL DIODES ARE CD6262

LIST OF MATERIALS

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

		DRAWN P. Peralta 9-2-65	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	ESTRON DONNER CORPORATION CONCORD CALIFORNIA
		CHECK [illegible]	DATE		
		ENGR. [illegible]	DATE	DECIMAL TOLERANCE	SCHEMATIC, RAMP GEN.
1259	17411	MECH	DATE	X ———	
1453	17411	PROJECT	DATE	.XX ———	
1264	17-411	APPROV	DATE	.XXX ———	
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE B	MATERIAL
APPLICATION				SHT 1 OF 1	DWG NO 17402 ISSUE D

5-17



MODEL 1253 OSCILLATOR LAYOUT

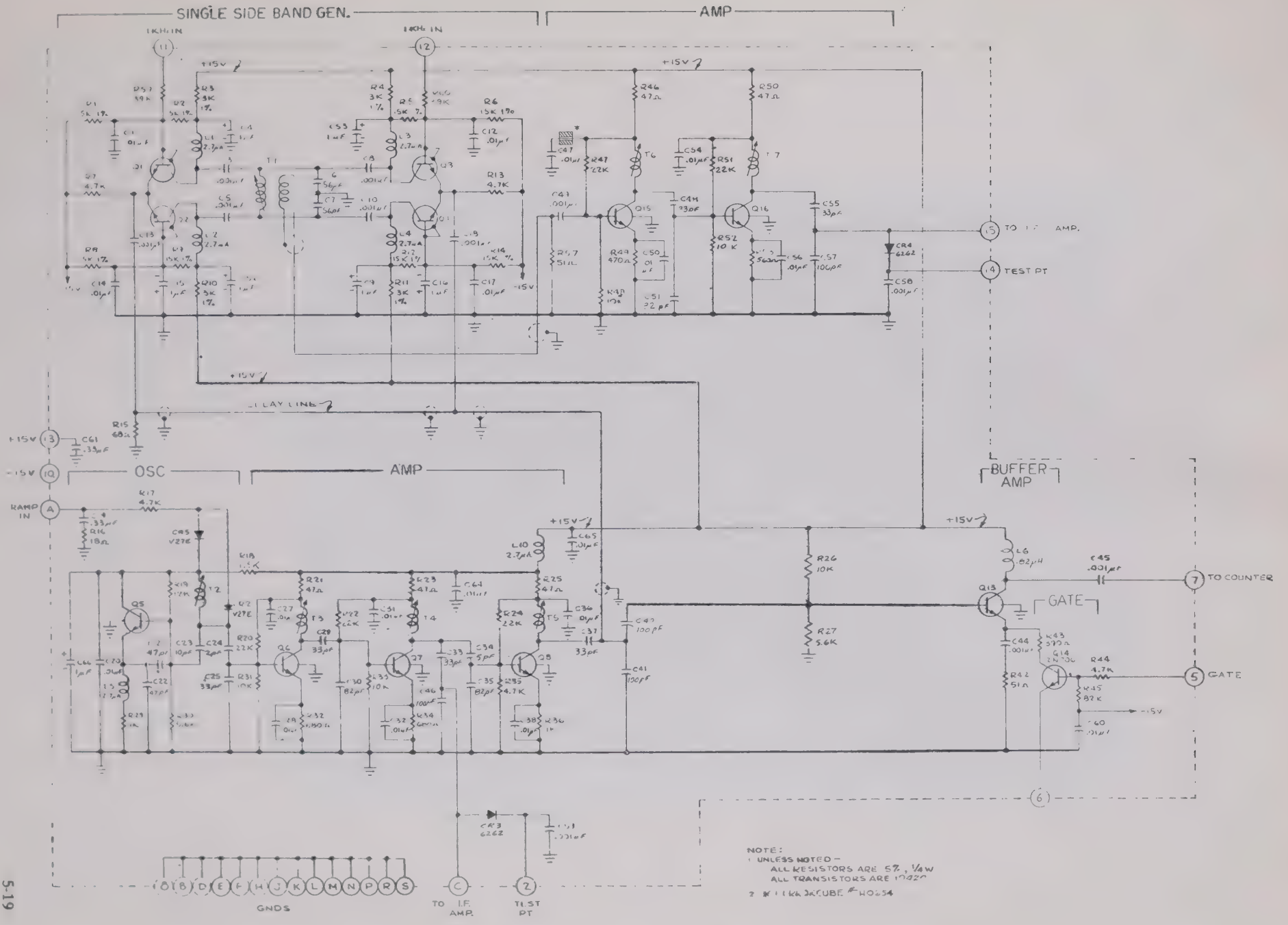
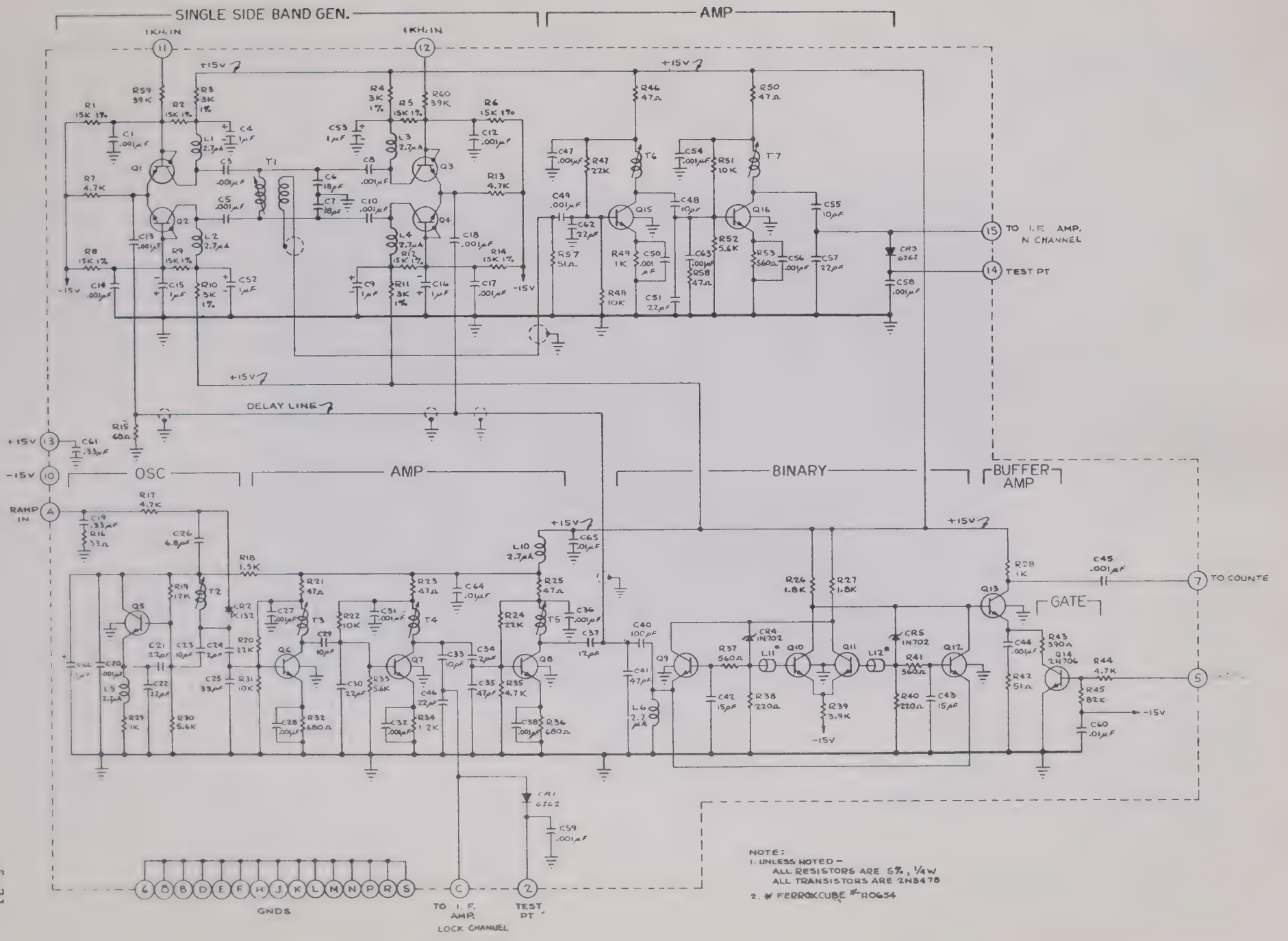
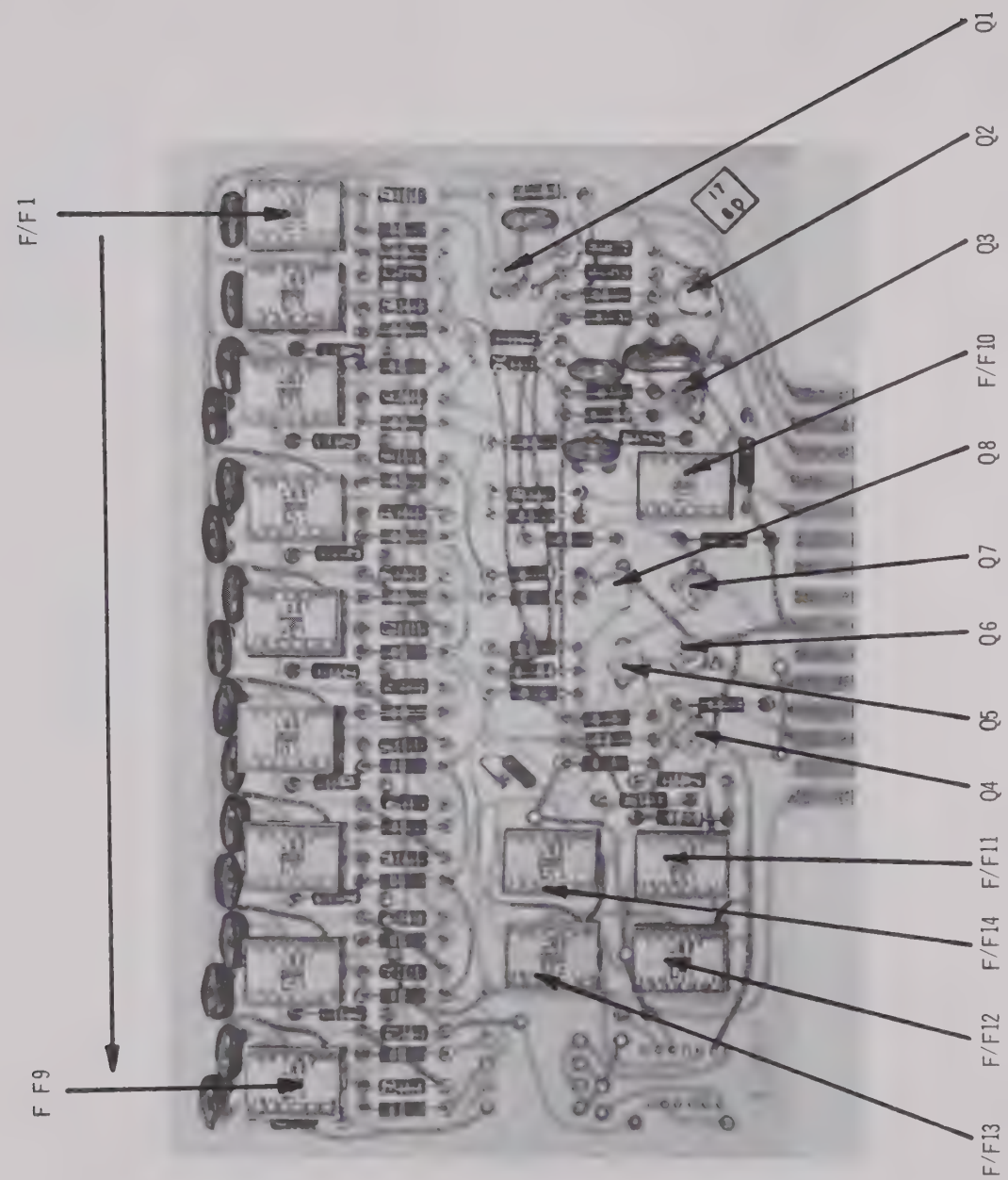


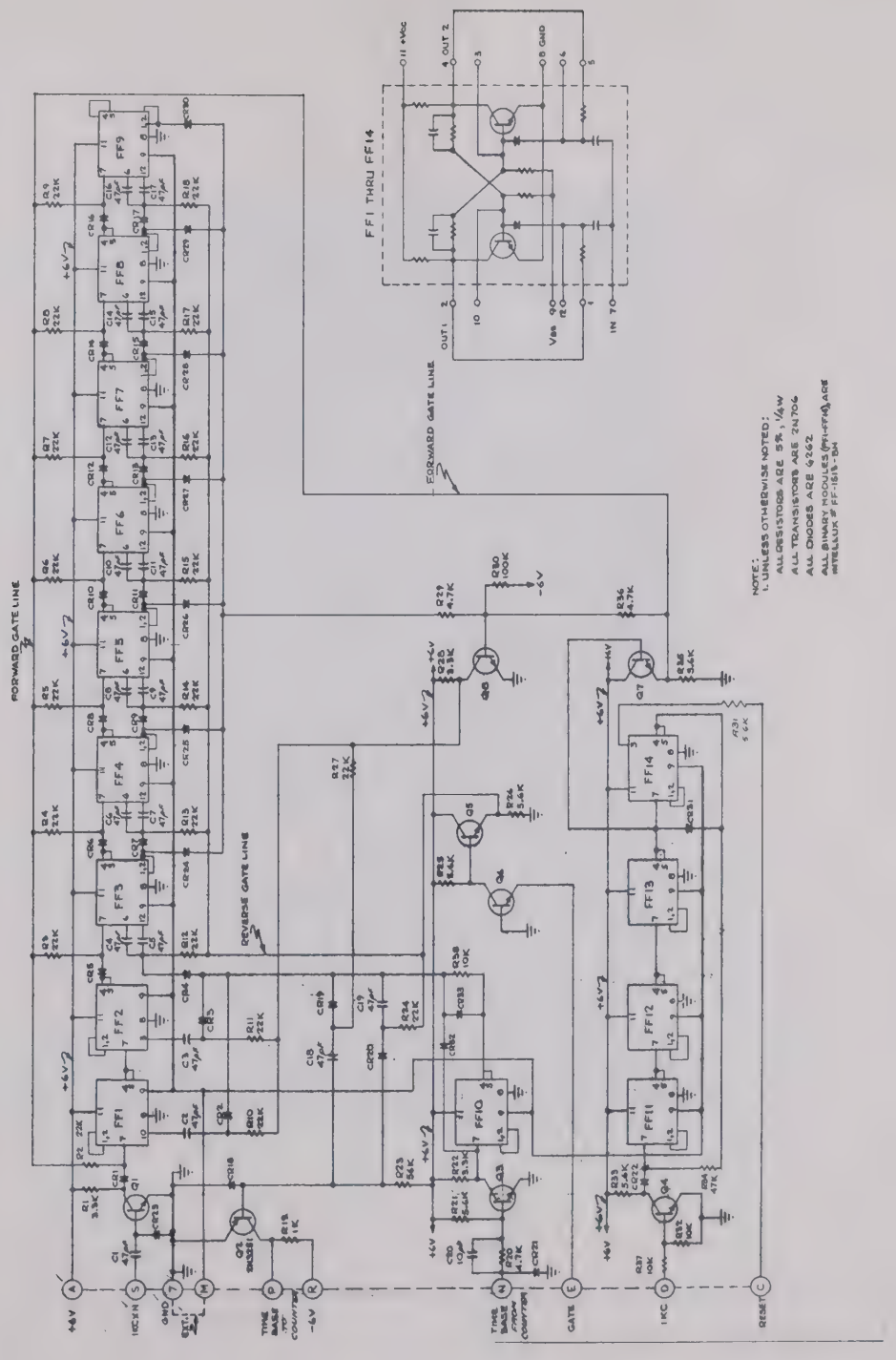
FIGURE 4-11 OSCILLATOR SCHEMATIC

1254/5 OSCILLATOR

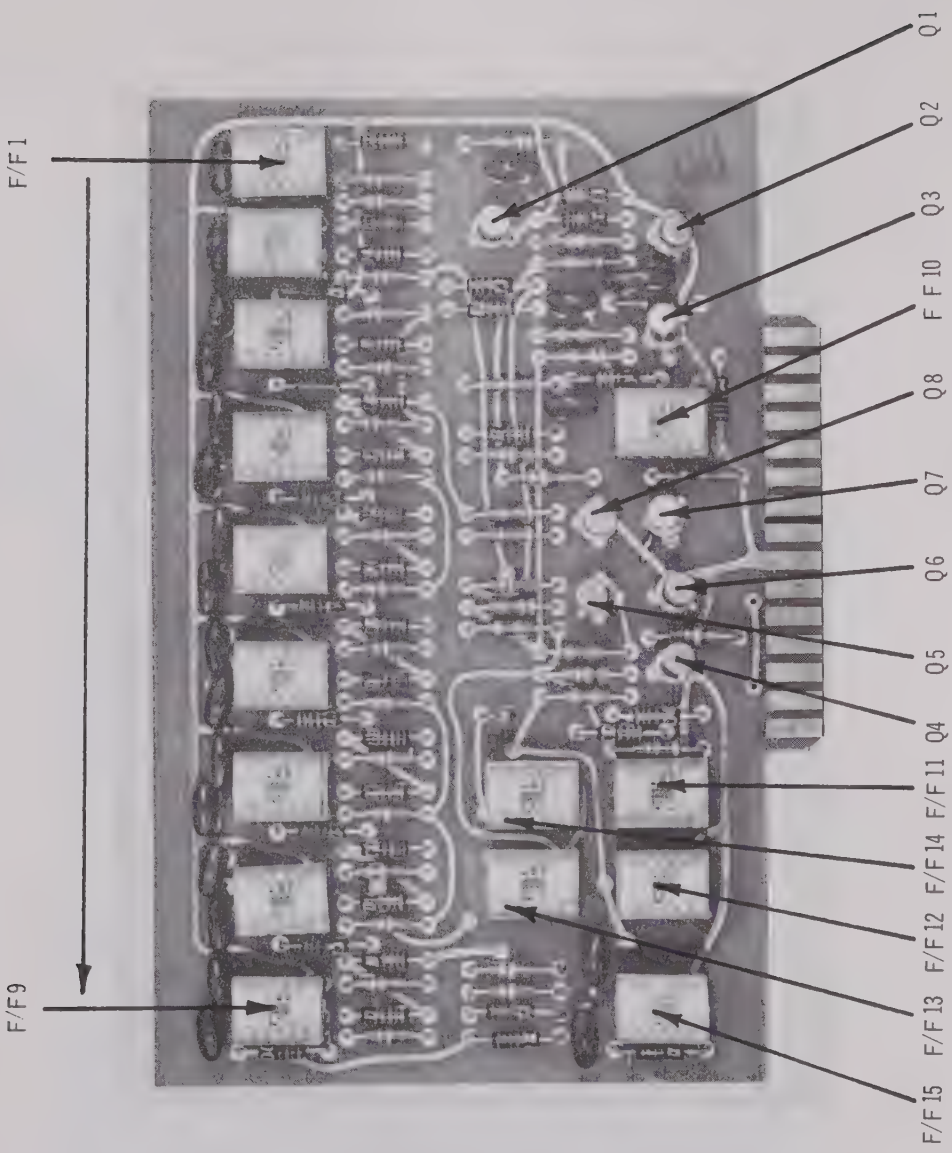

SINGLE SIDE BAND GEN.
AMP
1KH. IN
1KH. IN
+15V
+15V
+15V
+15V
DELAY LINE
-15V
-15V
OSC
AMP
BINARY
BUFFER AMP
RAMP IN
GATE
TO I.F. AMP, N CHANNEL
TEST PT
TO COUNTE
GNDS
TO I. F. AMP. LOCK CHANNEL
TEST PT
NOTE:
1. UNLESS NOTED – ALL RESISTORS ARE 5%, 1/4W ALL TRANSISTORS ARE 2N3478
2. * FERROXCUBE #10634

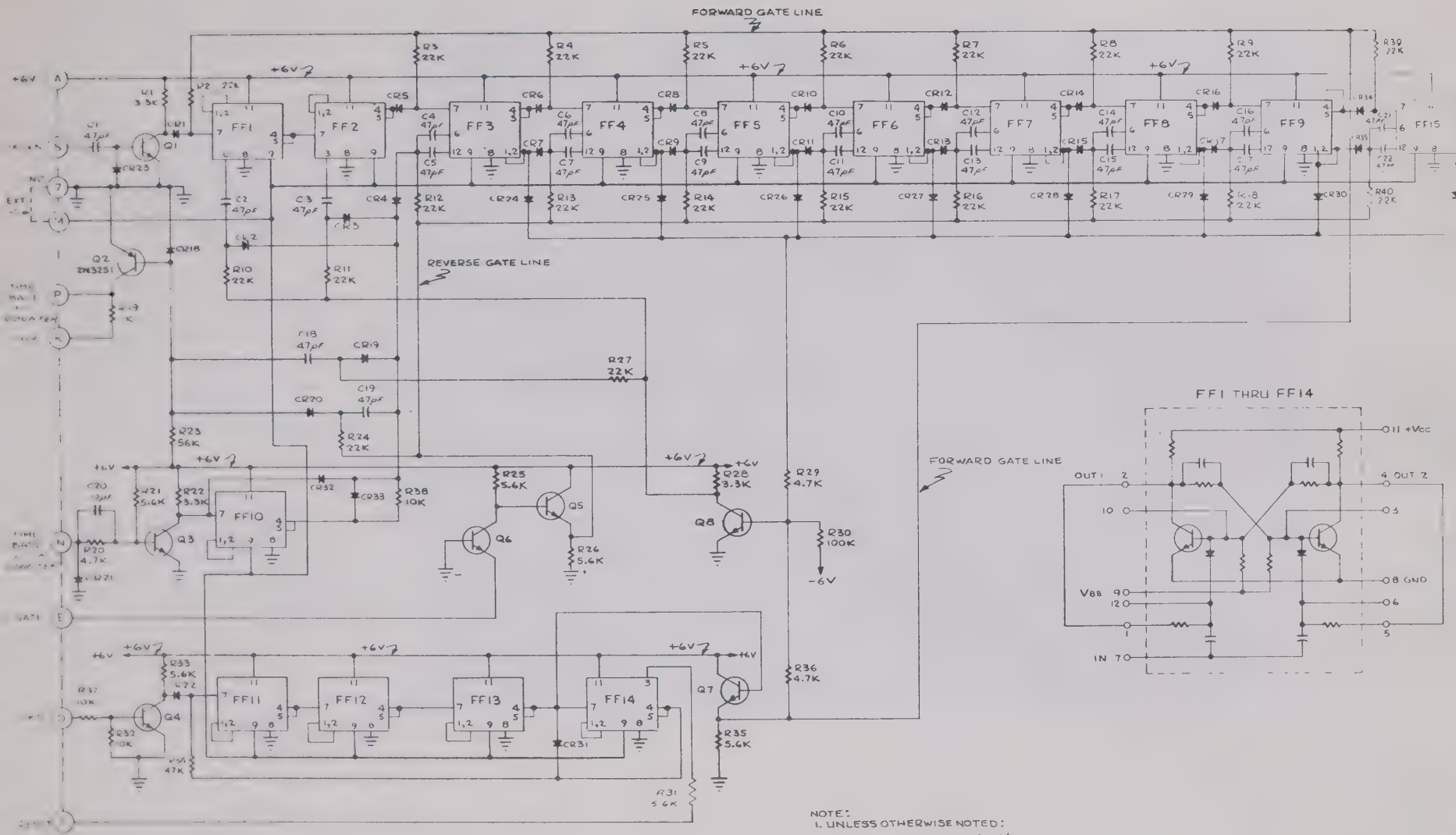


MODEL 1254 N COMPUTER LAYOUT



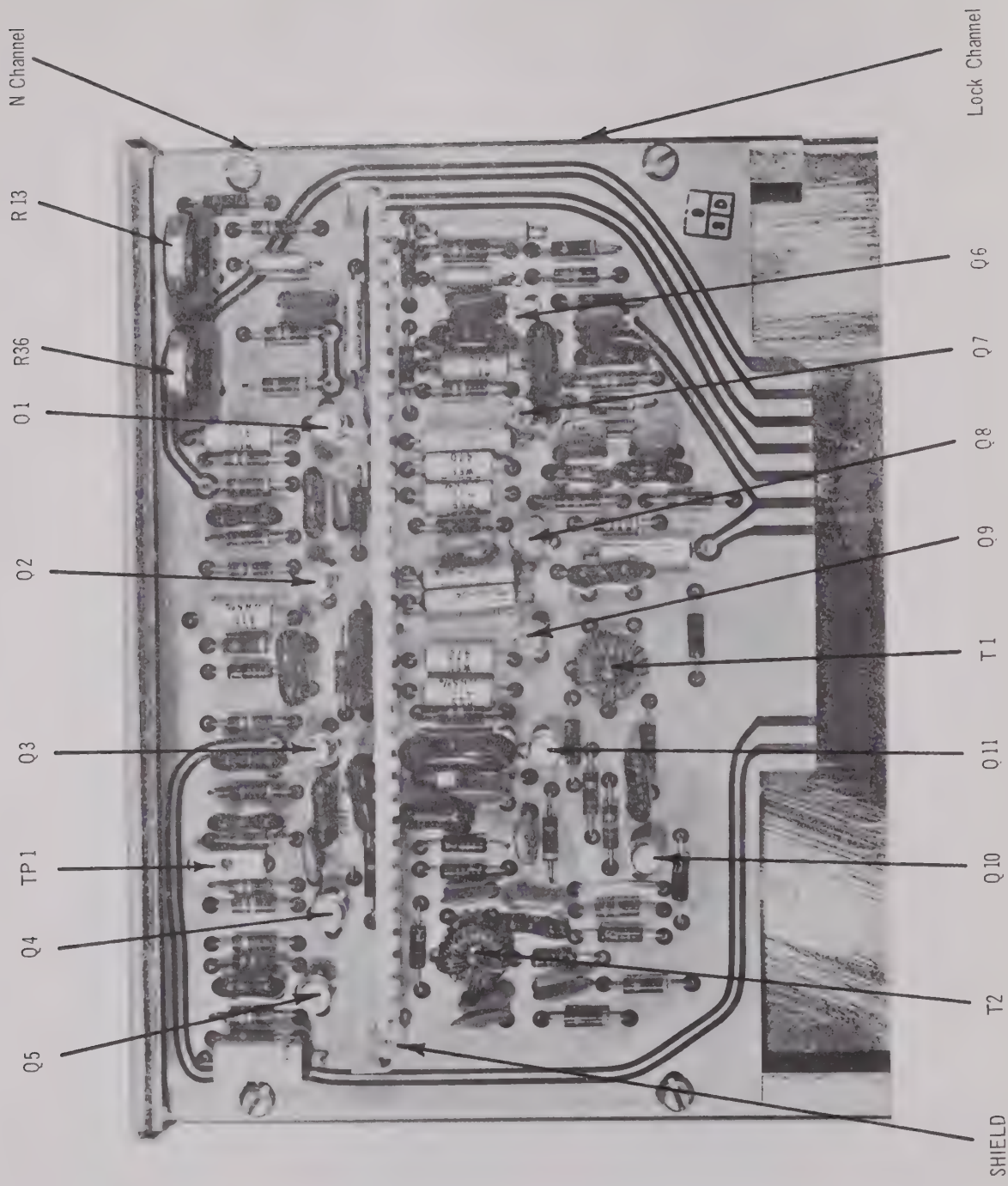
MODEL 1254 N COMPUTER SCHEMATIC


F/F 1
F/F 9
Q1
Q2
Q3
F F 10
Q8
Q7
Q6
Q5
Q4
F/F 11
F/F 14
F/F 12
F/F 13
F/F 15

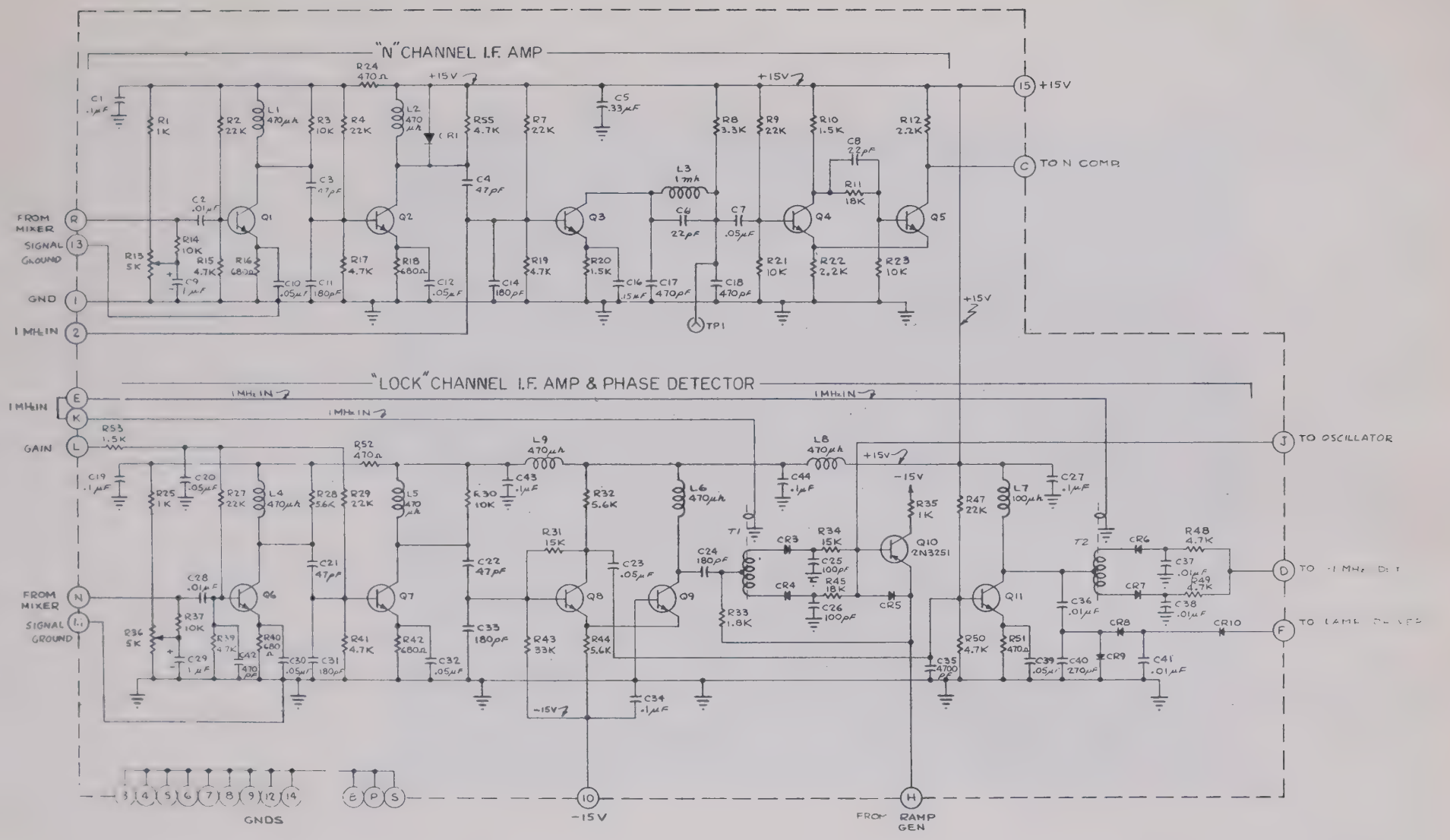


NOTE:
1. UNLESS OTHERWISE NOTED:
   ALL RESISTORS ARE 5%, 1/4W
   ALL TRANSISTORS ARE 2N706
   ALL DIODES ARE 6262
   ALL BINARY MODULES (FF1-FF14) ARE INTELLUX # FF-1513-BH

MODEL 1255 N COMPUTER SCHEMATIC

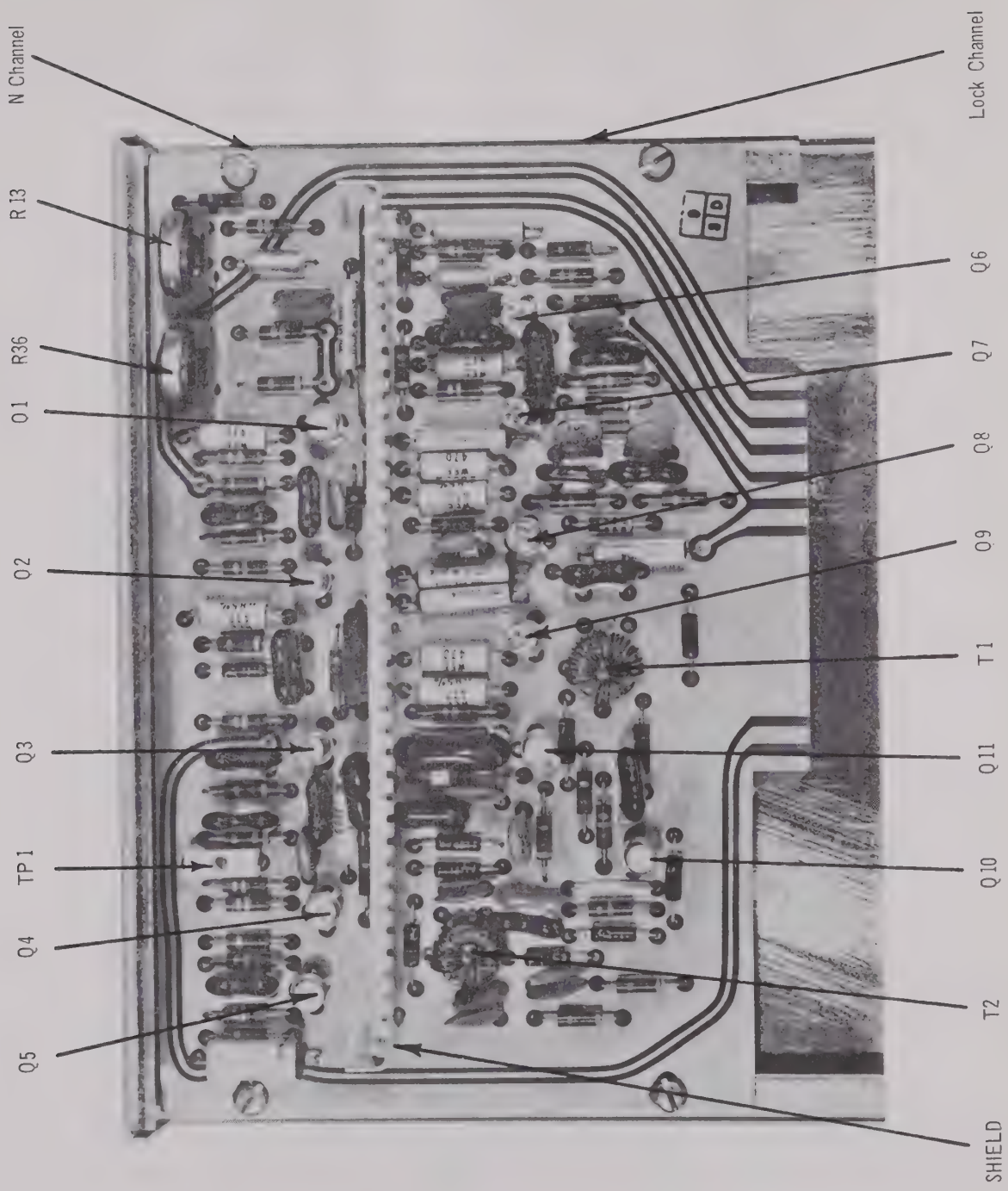


MODEL 1253 IF AMPLIFIER LAYOUT

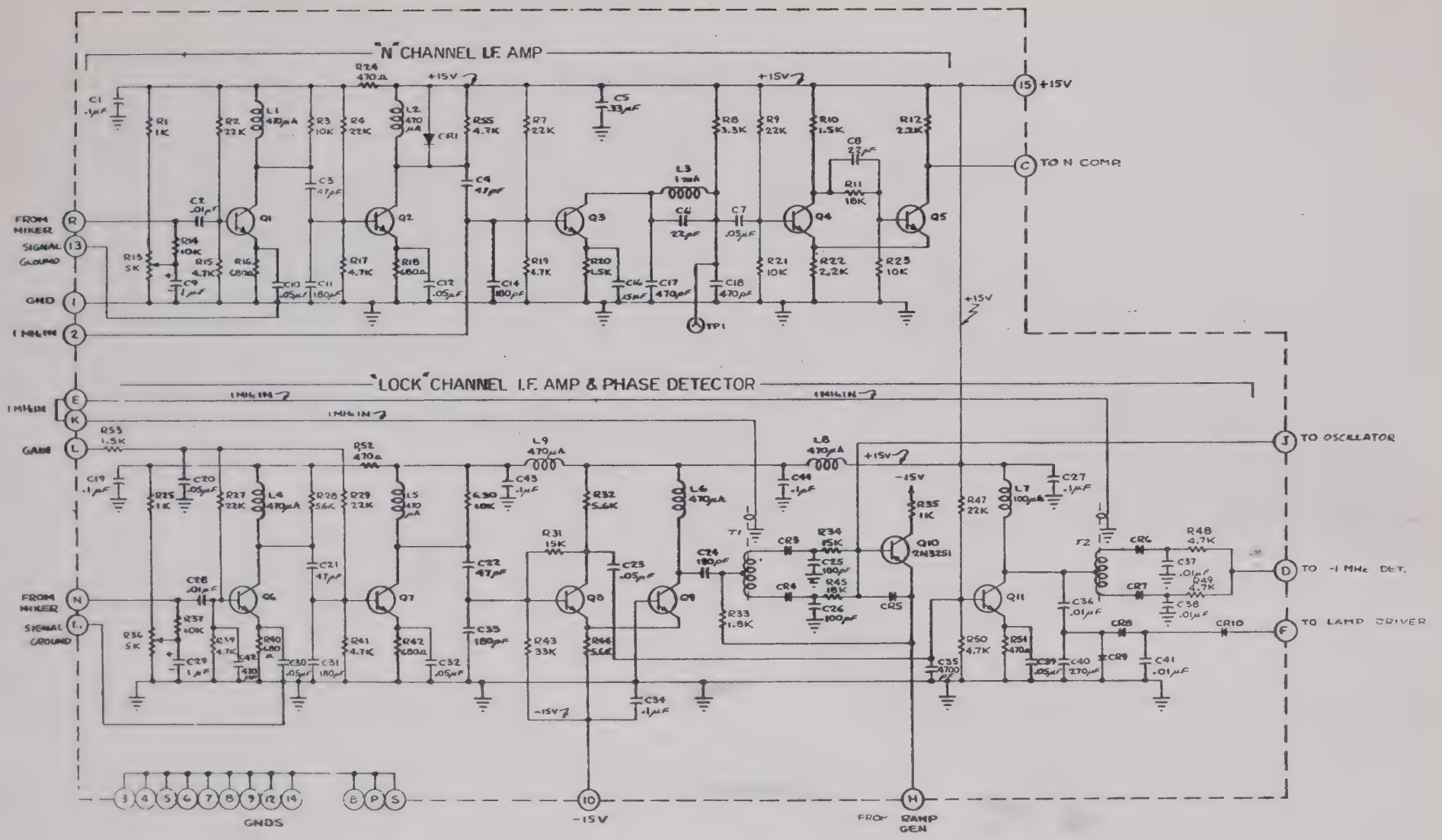


NOTE:
1. UNLESS NOTED—
ALL RESISTORS ARE 5%, ½W
ALL TRANSISTORS ARE 2N706
ALL DIODES ARE CD6262

MODEL 1253 IF AMPLIFIER SCHEMATIC



MODEL 1254 and 1255 IF AMPLIFIER LAYOUT



NOTE:
1. UNLESS NOTED—
ALL RESISTORS ARE 5%, ½W
ALL TRANSISTORS ARE 2N706
ALL DIODES ARE CD6262

MODEL 1254 and 1255 IF AMPLIFIER SCHEMATIC

MASTER PARTS LIST			
SYS-DON PART NO.	DESCRIPTION	MANUFACTURER	MFR PART NO.
C0233	CAPACITOR, 0.01 uf 150 v +60 -40%, ceramic disc	Central Lab.	DDM103
C0236	CAPACITOR, 0.1 uf 100 v 20%, paper-metal	Electron Prod	M1-104
C0237	CAPACITOR, 0.15 uf 100 v ±20%, paper-metal	Electron Prod	M1-154
C0239	CAPACITOR, 0.33 uf 100 v 20%, metalized mylar	Electron Prod	M1-334
C0261	CAPACITOR, 2 pf 500 v 10%, ceramic disc	Scottie	TSD402M
C0371	CAPACITOR, 22 uf 25 v 20%, tantalum	Sprague	109-D-226 x 0025C2
C0378	CAPACITOR, 22 pf 500 v 5%, dipped silver mica	Cornell Dubilier	CD-15-C-220-J
C0424	CAPACITOR, 0.001 uf 500 v 20%, ceramic disc	RMC	TYPE B
C0524	CAPACITOR, 1 uf 35 vdc, 20%, electrolytic, tantalum	T.I.	SCM105FP035D4
C0527	CAPACITOR, 10 pf 500 v 10%, dipped silver mica	El Menco	DM15C100K500V
C0528	CAPACITOR, 15 pf 500 v ±10%, dipped silver mica	El Menco	DM15C150K500V
C0531	CAPACITOR, 33 uf 500 v 10%, dipped silver mica	El Menco	DM15C330K500V
C0533	CAPACITOR, 47 pf 500 v 10%, dipped silver mica	El Menco	DM15E470K500V
C0534	CAPACITOR, 56 pf 500 v 10%, dipped silver mica	El Menco	DM15E560K500V
C0535	CAPACITOR, 82 pf 500 v 10%, dipped silver mica	El Menco	DM15820K500V
C0536	CAPACITOR, 100 pf 500 v 10%, dipped silver mica	El Menco	DM15F101K500V
C0539	CAPACITOR, 270 pf 500 v 10%, dipped silver mica	El Menco	DM15F271K500V
C0542	CAPACITOR, 470 pf 300 v 10%, dipped silver mica	El Menco	DM15F471K500V
C0562	CAPACITOR, 0.01 uf 50 v ±20%, ceramic disc	Sprague	19C214
C0596	CAPACITOR, 5 pf 500 v 5%, dipped silver mica	El Menco	DM15C050K500V
C0633	CAPACITOR, 4700 pf 300 v 5%, dipped silver mica	El Menco	DM20F472J300V
C0635	CAPACITOR, 68 pf 500 v 10%, dipped silver mica	El Menco	DM15E680K500V
C0637	CAPACITOR, 12 pf 500 v 10%, dipped silver mica	El Menco	DM15C120K500V
C0644	CAPACITOR, 560 pf 300 v ±10%, dipped silver mica	El Menco	DM15E561K500V
C0672	CAPACITOR, 0.05 uf 12 v, ceramic disc	RMC	MAGNACAP

MASTER PARTS LIST (Continued)

SYS-DON PART NO.	DESCRIPTION	MANUFACTURER	MFR PART NO.
C0697	CAPACITOR, 18 pf 500 v 10%, dipped silver mica	El Menco	DM10180K500V
C0699	CAPACITOR, 0.022 uf 200 v 2%, mylar	Sprague	192P22302
C0701	CAPACITOR, 0.33 uf, metalized mylar, epoxy case	Electron Prod	DE2-334
C0707	CAPACITOR, 180 pf 300 v 5%, dipped silver mica	El Menco	DM15F181J
C0737	CAPACITOR, 0.015 uf 200 v 10%, mylar	Sprague	192P15392
C0826	CAPACITOR, 0.033 uf 200 v 210%, mylar	Sprague	192P33392
C0848	CAPACITOR, 47 pf 500 v 10%, dipped silver mica	El Menco	DM10470J
C0489	CAPACITOR, 6.8 pf 10% 1000 v	Arco	CCTO-6R8
C0851	CAPACITOR, 1047 uf 200 v 10%, mylar	Sprague	192P47392
C0852	CAPACITOR, 0.01 uf 200 v 210%, mylar	Sprague	192P10392
C0853	CAPACITOR, 0.0047 pf 200 v 210%	Sprague	192P47292
CR0126	DIODE, Zener 2-3.2 v	Hoffman	IN702
CR0150	DIODE	Continental Device	CD6262
CR0227	DIODE, Sealed reversible, demountable base	Microwave	MA 458D
CR0244	DIODE, PC-132	TRW	PC132
CR0261	DIODE	Hewlett-Packard Association	HPA0112
CR0269	DIODE, Step recovery	Microwave	HPA0151
CR0271	DIODE, 65 v 4 v=27 pf	TRW	V27E
CR0273	DIODE, IN831	Sylvania	IN831
CR0307	DIODE, Zener, 15 v 3/4 w		1N3683B
E0100	TERMINAL SPADE LUG	USECO	NO. 2000B
E0130	INSULATOR, Cover	Duralith PVC	
E0140	STANDOFF, Insulated	USECO	1486B
E0201	BINARY MOD., Intellux FF-15-3-BH	Intellux	FF-15-3-BH
E0203	CORE, (Ferroxcube 266 T125/ 3E2A)	Ferrox Cube	266 T125/3E2A
E0223	COIL FORM, 3623-2 Cambion	Cambion	3623-2, .3401G x .375 WIDE
H0494	TERMINAL STRIP	Cinch	52A (3-TERMINAL)
H0654	FERRITE CORE	Ferrox Cube	56-590-65/20-3B
H1298	KNOB	Raytheon	70-1WD-1G

MASTER PARTS LIST (Continued)

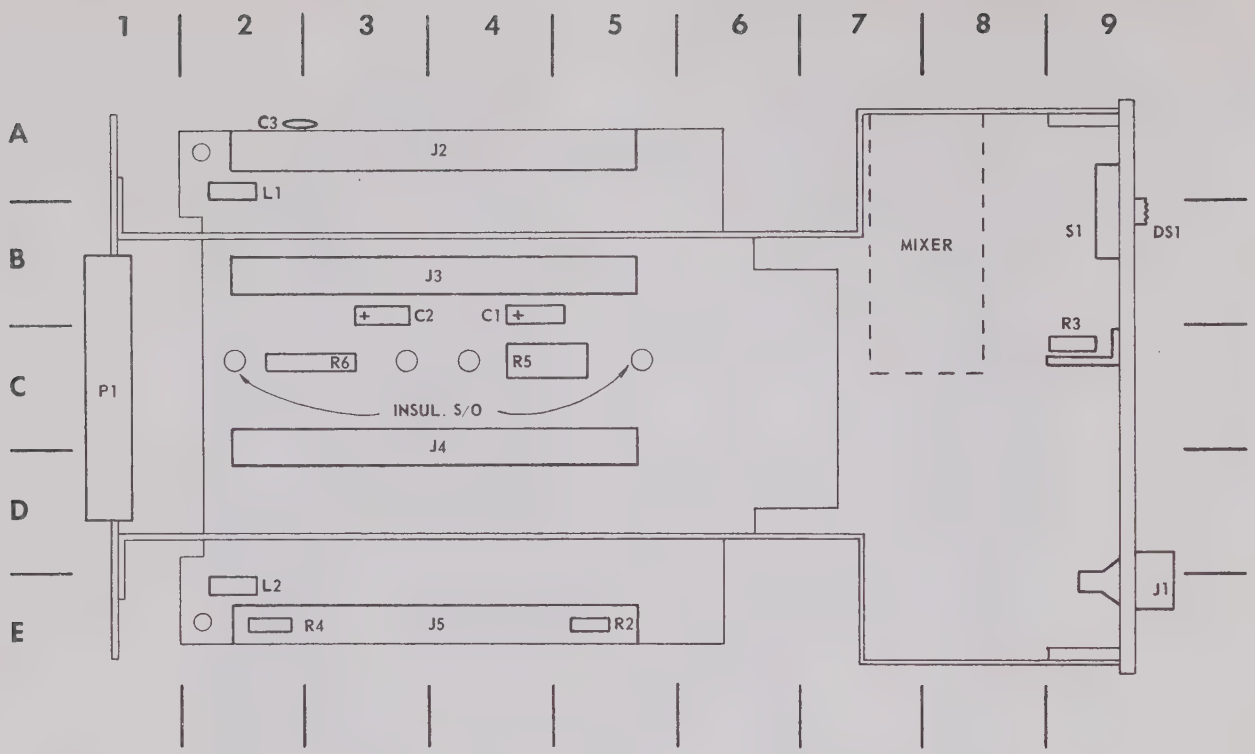
SYS-DON PART NO.	DESCRIPTION	MANUFACTURER	MFR PART NO.
I0061	BULB, Neon	Eldema	B9ACNE2 (+ SYMBOL)
J0261	CONNECTOR, 50 pin, male	Amphenol	57-10500
J0308	CONNECTOR, min. coax	Auto-metal	801B1800
J0324	CONNECTOR, 30 pin, female	Viking	VH15/1AN5
J0325	CONNECTOR, OSM	Omni-Spectra	OSM501-2
J0326	CONNECTOR, N to OSM	Omni-Spectra	21310
J0344	CONNECTOR, Male phono	Cinch	202-11-01-061
L0019	CHOKE, 470 uh	Nytronics	WEE 470
L0048	CHOKE, 2.7 uh, Wee ductor 2.7	Bell Electronic	WEE 2.7 UH
L0059	CHOKE, 0.82 uh, 1300 ua	RFC50.82	ESSEX
L0067	CHOKE, 270 uh	Stanwyck	DINK 270
L0068	CHOKE, 1000 uh	Stanwyck	DINK 1,000
L0073	CHOKE, 100 uh	Stanwyck	DINK 100
L0074	CHOKE, 47 uh	National	NA 471
Q0130	TRANSISTOR, 2N706	Philco	2N706
Q0174	TRANSISTOR, 2N3251	Motorola	2N3251
Q0177	TRANSISTOR, 2N3478	RCA	2N3478
R0693	RESISTOR, 5.1 K 5% 1/4 w	Allen Bradley	CB5125
R0697	RESISTOR, 220 K 5% 1/4 w	Allen Bradley	CB2245
R0728	RESISTOR, 15 K 5% 1/4 w	Allen Bradley	CB1535
R0741	RESISTOR, 100 K 5% 1/4 w, Carbon comp	Allen Bradley	CB1045
R0742	RESISTOR, 3.3 K 5% 1/4 w, Carbon comp	Allen Bradley	CB3325
R0743	RESISTOR, 47Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB4705
R0748	RESISTOR, 39 K 5% 1/4 w, Carbon comp	Allen Bradley	CB3935
R0749	RESISTOR, 2.2 K 5%, 1/4 w	Allen Bradley	CB2225
R0759	RESISTOR, 12 K 5% 1/4 w, Carbon comp	Allen Bradley	CB1235
R0760	RESISTOR, 220Ω 5% 1/4 w	Allen Bradley	CB2215
R0762	RESISTOR, 820Ω 5% 1/4 w	Allen Bradley	CB8215
R0765	RESISTOR, 1 K 5% 1/4 w, Carbon comp	Allen Bradley	CB1025
R0766	RESISTOR, 10 K 5% 1/4 w, Carbon comp	Allen Bradley	CB1035
R0768	RESISTOR, 22 K 5% 1/4 w, Carbon comp	Allen Bradley	CB2235
R0777	RESISTOR, 47 K 5% 1/4 w, Carbon comp	Allen Bradley	CB4735

MASTER PARTS LIST (Continued)

SYS-DON PART NO.	DESCRIPTION	MANUFACTURER	MFR PART NO.
R0780	RESISTOR, 0.33 K 5% 1/4 w	Allen Bradley	CB3335
R0783	RESISTOR, 1.5 K 5% 1/4 w, Carbon comp	Allen Bradley	CB1525
R0784	RESISTOR, 82 K 5% 1/4 w, Carbon comp	Allen Bradley	CB8235
R0785	RESISTOR, 18 K 5 % 1/4 w	Allen Bradley	CB1835
R0809	RESISTOR, 1.2 K 5% 1/4 w	Allen Bradley	CB1225
. .19	RESISTOR, 560Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB5615
R0821	RESISTOR, 560Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB5615
R0824	RESISTOR, 27 K 5% 1/4 w	Allen Bradley	CB2735
R0880	RESISTOR, 390Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB3915
R0883	RESISTOR, 8.2 K 5% 1/4 w	Allen Bradley	CB8225
R0892	RESISTOR, 4.7 K 5% 1/4 w, Carbon comp	Allen Bradley	CB4725
R0939	RESISTOR, 3.9 K 5% 1/4 w, Carbon comp	Allen Bradley	CB3925
R0959	RESISTOR, 1.8 K 5% 1/4 w	Allen Bradley	CB1825
R0961	RESISTOR, 150 K 5% 1/4 w	Allen Bradley	CB1545
R0966	RESISTOR, 100Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB1015
R0967	RESISTOR, 220 K 5% 1/4 w, Carbon comp	Allen Bradley	CB2245
R1044	RESISTOR, 470Ω 5% 1/4 w	Allen Bradley	CB4715
R1234	RESISTOR, 680Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB6815
R1235	RESISTOR, 56 K 5% 1/4 w, Carbon comp	Allen Bradley	CB5635
R1246	RESISTOR, 51Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB5105
R1426	RESISTOR, 68Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB6805
R1550	RESISTOR, 33Ω 5% 1/4 w, Carbon comp	Allen Bradley	CB3305
R1580	RESISTOR, 680Ω 5% 2 w, Carbon comp	Allen Bradley	CB6805
R1674	RESISTOR, 100Ω 5% 5 w	Sprague	243-E 1015
R1860	POTENTIOMETER, 10 K Panel MT	Mallory	70-08632-3
R2073	RESISTOR, 15 K 1% 1/4 w, Wire wound	Electra	MF5CD
R2074	RESISTOR, 3 K 1% 1/4 w, Wire wound	Electra	MF5CD
R2076	RESISTOR, 5 K, Trimpot Spectrol	Spectrol No. 85	NO. 85
R2190	RESISTOR, 130Ω 1% 3 w, Wire wound	Ohmite	884

MASTER PARTS LIST (Continued)

SYS-DON PART NO.	DESCRIPTION	MANUFACTURER	MFR PART NO.
RF0002	T PAD, 10DB, 1/4 w	EMC Tech.	TS-0016M10DB
RF0003	HYBRID JUNCTION	Sage	7754-3
RF0004	RESISTOR, Sheet	Mylohm	
S0110	SWITCH, DPDT	Stackpole	SS50
15850	TRANSISTOR	Per S-D Spec.	
17636	TRANSFORMER	Per S-D Spec.	
17637	TRANSFORMER, Phase detector	Per S-D Spec.	
19070	TRANSFORMER	Per S-D Spec.	
19191-1	TRANSFORMER	Per S-D Spec.	
19191-2	TRANSFORMER	Per S-D Spec.	
19191-3	TRANSFORMER	Per S-D Spec.	
19420	TRANSISTOR	Per S-D Spec.	



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	B4	C0371
C2	B3	
C3	A2	C0562
CR1	MIXER	CR0273
CR2	MIXER	CR0261
CR3	MIXER	
CR4	MIXER	
CR5*		CR0307
***	MIXER	CR0269
**	MIXER	CR0227
DS1	B9	I0061
E1	MIXER	H0654
E2	MIXER	
J1	E9	J0326
J2	A3	J0324
J3	B3	
J4	C3	
J5	E5	
		J0308

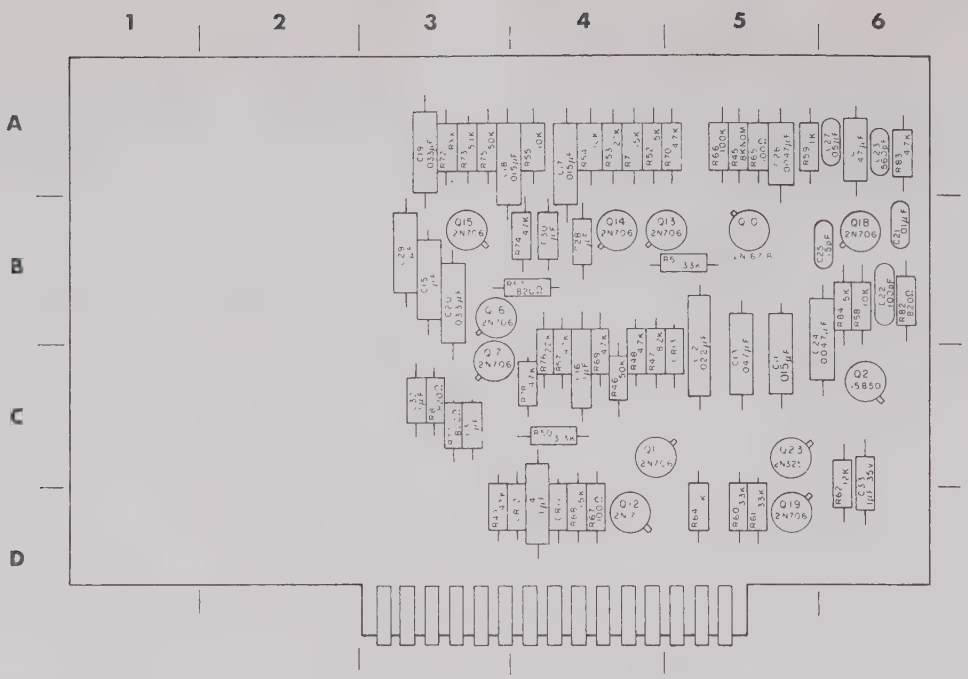
REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
L1	A2	L0067
L2	E2	
P1	C1	J0261
P6	MIXER	J0344
P7	MIXER	
P8	MIXER	
P9	MIXER	
P10		J0325
R1	E9	R1860
R2	E5	R0743
R3	C9	R0697
R4	E2	
R5	C4	R1580
R6*	C3	R2190
R6***	C3	R1674
RF1	MIXER	RF0002
RF2	MIXER	
***	MIXER	RF0004
**	B9	RF0003

ACTO Chassis Assembly, Models 1253, 1254 and 1255 (Sheet 1 of 2)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
S1		S0110
		E0130
	D9	H1298

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
	C9	HO494
	C2, 5	EO140

ACTO Chassis Assembly, Models 1253, 1254 and 1255 (Sheet 2 of 2)



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C11	C5	C0737
C12	C5	C0699
C13	C5	C0851
C14	D4	C0236
C15	B3	C0236
C16	B4	C0236
C17	A4	C0737
C18	A4	C0737
C19	A3	C0826
C20	B3	C0826
C21	B6	C0233
C22	B5	C0536
C23	A6	C0644
C24	C5	C0853
C25	B6	C0528
C26	A5	C0853
C27	A6	C0672
C28	B4	C0524
C29	B3	C0236
C30	B4	C0524
C31	C3	C0524
C32	C3	C0524

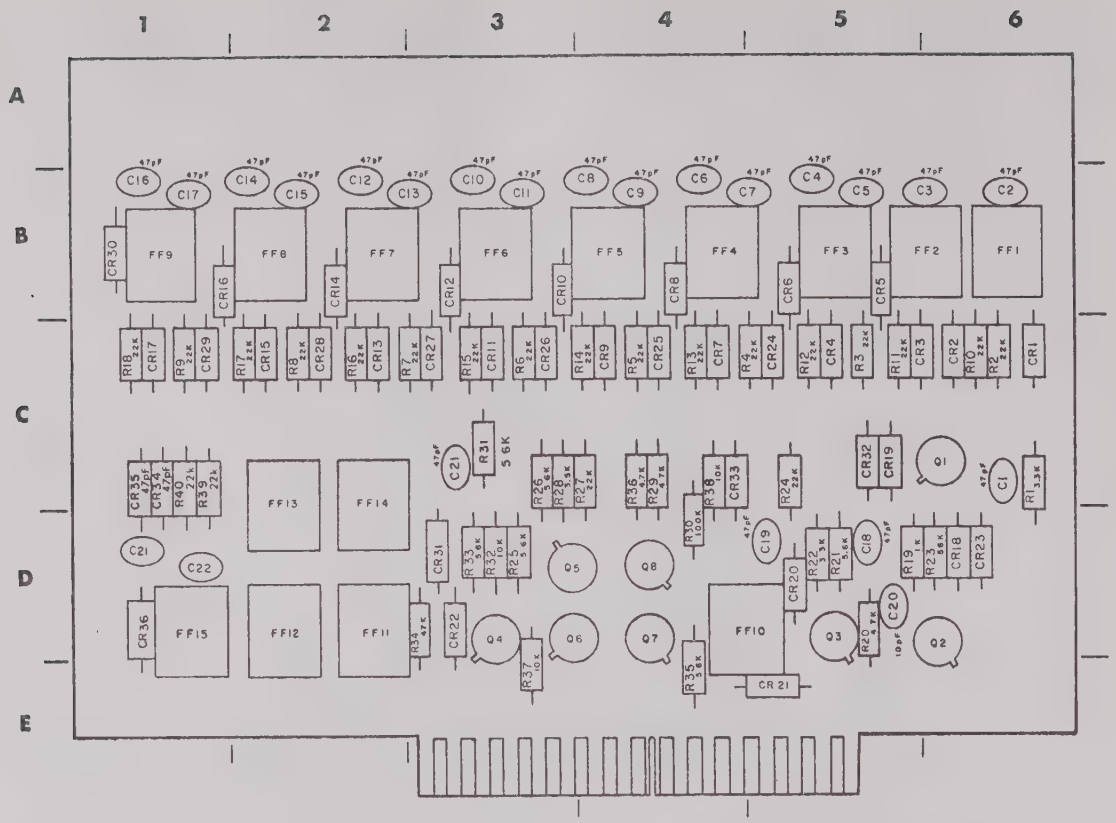
REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C33	D5	C0524
CR11	D4	CR0150
CR12	D3	CR0150
CR13	C5	CR0150
L1	A6	L0074
R45	A5	RXXXX
R46	C4	R0961
R47	C4	R0883
R48	C4	R0892
R49	D3	R0892
R50	C4	R0742
R51	B5	R0780
R52	A4	R0728
R53	A4	R0824
R54	A4	R0766
R55	A4	R0766
R56	C4	R0777
R57	B4	R0762
R58	B6	R0766
R59	A5	R0765
R60	D5	R0780
R61	D5	R0742

Ramp Generator, PC Board Assembly, Models 1253 and 1254
(Sheet 1 of 2)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R62	D6	R0759
R63 N/A		
R64	D5	R0765
R65	A5	R0966
R66	A5	R0741
R67	D4	R0966
R68	D4	R0728
R69	C4	R0777
R70	A5	R0892
R71	A4	R0728
R72	A3	Selectable
R73	A3	R0693
R74	B4	R0777
R75	A3	R0961
R76	C4	R0768
R77	C3	R0762
R78	C4	R0892
R79 N/A		
R80	C3	R0762

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R81 N/A		
R82	B6	R0762
R83	A6	R0892
R84	B6	R0783
R85 N/A		
R86 N/A		
Q10	B5	Q0084
Q11	C4	Q0130
Q12	D4	Q0130
Q13	B4	Q0130
Q14	B4	Q0130
Q15	B3	Q0130
Q16	B3	Q0130
Q17	C3	Q0130
Q18	B6	Q0130
Q19	D5	Q0130
Q21	C6	15850
Q22 N/A		
Q23	C5	Q0174

Ramp Generator, PC Board Assembly, Models 1253 and 1254
(Sheet 2 of 2)



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	C6	C0848
C2	B6	C0848
C3	B5	C0848
C4	B5	C0848
C5	B5	C0848
C6	B4	C0848
C7	B4	C0848
C8	B4	C0848
C9	B4	C0848
C10	B3	C0848
C11	B3	C0848
C12	B2	C0848
C13	B3	C0848
C14	B2	C0848
C15	B2	C0848
C16	B1	C0848
C17	B1	C0848
C18	D5	C0848

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C19	D5	C0848
C20	E5	C0527
C21*	D1	C0848
C22*	D1	C0848
CR1	C6	CR0150
CR2	C6	CR0150
CR3	C5	CR0150
CR4	C5	CR0150
CR5	B5	CR0150
CR6	B5	CR0150
CR7	C4	CR0150
CR8	B4	CR0150
CR9	C4	CR0150
CR10	B3	CR0150
CR11	C3	CR0150
CR12	B3	CR0150
CR13	C2	CR0150
CR14	B2	CR0150

*Model 1255 only.

"N" Computer, PC Board Assembly, Models 1253, 1254 and 1255
(Sheet 1 of 3)

REFERENCE DESIGNATION	COMPONENT LOCATION	S-D PART NO.
CR15	C2	CR0150
CR16	B1	CR0150
CR17	C1	CR0150
CR18	D6	CR0150
CR19	C5	CR0150
CR20	D5	CR0150
CR21	E5	CR0150
CR22	E3	CR0150
CR23	D6	CR0150
CR24	C5	CR0150
CR25	C4	CR0150
CR26	C3	CR0150
CR27	C3	CR0150
CR28	C2	CR0150
CR29	C1	CR0150
CR30	B1	CR0150
CR31	D3	CR0150
CR32**	C5	CR0150
CR33**	C4	CR0150
CR34*	C1	CR0150
CR35*	C1	CR0150
CR36*	D1	CR0150
FF1	B6	E0201
FF2	B5	E0201
FF3	B5	E0201
FF4	B4	E0201
FF5	B4	E0201
FF6	B3	E0201
FF7	B2	E0201
FF8	B2	E0201
FF9	B1	E0201
FF10**	D4	E0201
FF11	D2	E0201
FF12	D2	E0201
FF13	C2	E0201
FF14	C2	E0201
FF15*	D1	E0201
R1	C6	R0742
R2	C6	R0768
R3	C5	R0768

REFERENCE DESIGNATION	COMPONENT LOCATION	S-D PART NO.
R4	C4	R0768
R5	C4	R0768
R6	C3	R0768
R7	C2	R0768
R8	C2	R0768
R9	C1	R0768
R10	C6	R0768
R11	C5	R0768
R12	C5	R0768
R13	C4	R0768
R14	C4	R0768
R15	C3	R0768
R16	C2	R0768
R17	C2	R0768
R18	C1	R0768
R19	D5	R0765
R20	E5	R0892
R21	D5	R0821
R22	D5	R0742
R23	D6	R1235
R24	C5	R0768
R25	D3	R0821
R26	C3	R0821
R27	C4	R0768
R28	C3	R0742
R29	C4	R0892
R30	D4	R0741
R31	N/A	R0741
R32	D3	R0766
R33	D3	R0821
R34	E2	R0777
R35	E4	R0821
R36	C4	R0892
R37	E3	R0766
R38**	C4	R0766
R39	C1	R0768
R40	C1	R0768
Q1	C5	Q0130
Q2	E5	Q0174
Q3	E5	Q0130

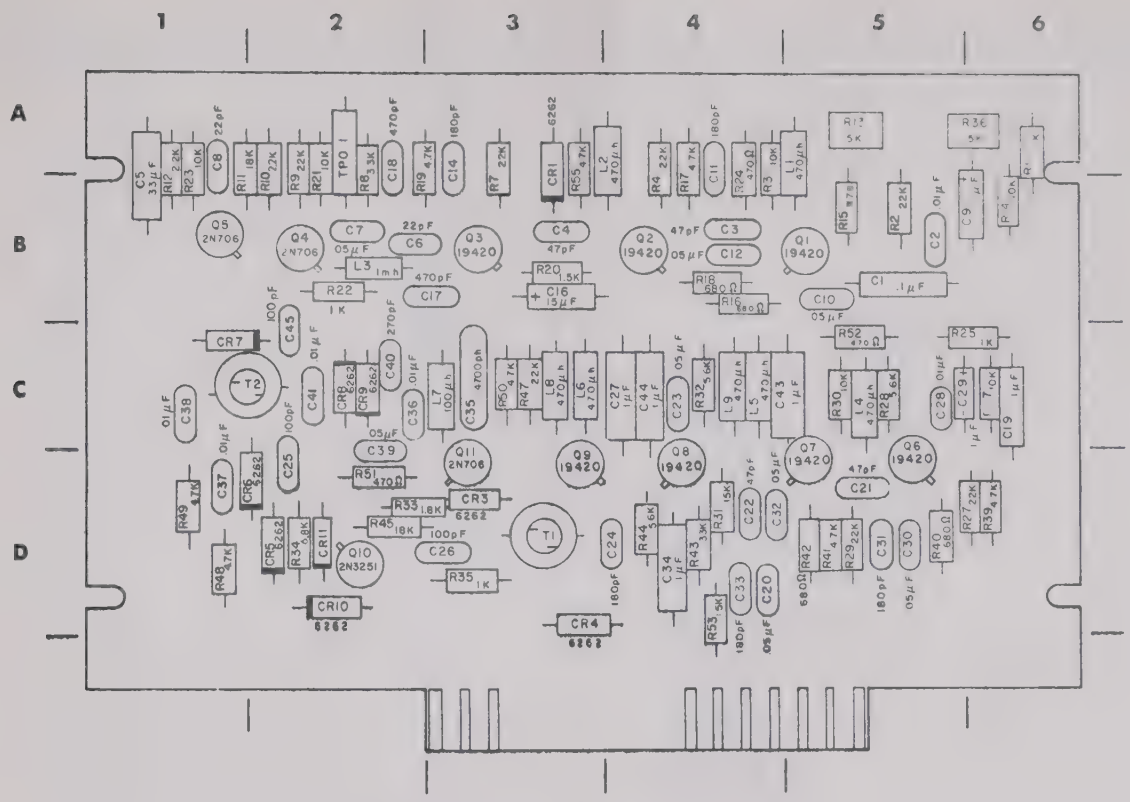
*Model 1255 only.
**Models 1254 and 1255 only.

"N" Computer, PC Board Assembly, Models 1253, 1254 and 1255
(Sheet 2 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q4	E3	Q0130
Q5	D3	Q0130
Q6	E3	Q0130

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q7	E4	Q0130
Q8	D4	Q0130

"N" Computer, PC Board Assembly, Models 1253, 1254 and 1255
(Sheet 3 of 3)



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	B5	C0236
C2	B5	C0233
C3	B4	C0533
C4	B3	C0533
C5	B1	C0239
C6	B2	C0378
C7	B2	C0672
C8	A1	C0378
C9	B6	C0524
C10	B5	C0672
C11	A4	C0707
C12	B4	C0672
C13	N/A	Not Used
C14	A3	C0707
C15	N/A	Not Used
C16	B3	C0524
C17	B2	C0542

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C18	A2	C0542
C19	C6	C0236
C20	D4	C0672
C21	D5	C0533
C22	D4	C0533
C23	C4	C0672
C24	D4	C0707
C25	C2	C0536
C26	D3	C0536
C27	C4	C0236
C28	C5	C0236
C29	C5	C0524
C30	D5	C0672
C31	D5	C0707
C32	D4	C0672
C33	D4	C0707
C34	D4	C0236

I. F. Amplifier, PC Board Assembly, Model 1253
(Sheet 1 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C35	C3	C0633
C36	C2	C0233
C37	D1	C0233
C38	C1	C0233
C39	C2	C0672
C40	C2	C0539
C41	C2	C0233
C42	N/A	
C43	C5	C0236
C44	C4	C0236
C45	C2	C0536
CR1	A3	CR0150
CR2	N/A	Not Used
CR3	D3	CR0150
CR4	D3	CR0150
CR5	D2	CR0150
CR6	D1	CR0150
CR7	C1	CR0150
CR8	C2	CR0150
CR9	C2	CR0150
CR10	D2	CR0150
CR11	D2	CR0150
L1	A5	L0019
L2	A3	L0019
L3	B2	L0068
L4	C5	L0019
L5	C4	L0019
L6	C3	L0019
L7	C3	L0073
L8	C3	L0019
L9	C4	L0019
R1	A6	R0765
R2	B5	R0768
R3	A4	R0766
R4	A4	R0768
R5	N/A	Not Used
R6	N/A	Not Used
R7	A3	R0768
R8	A2	R0742
R9	A2	R0768
R10	A2	R0749

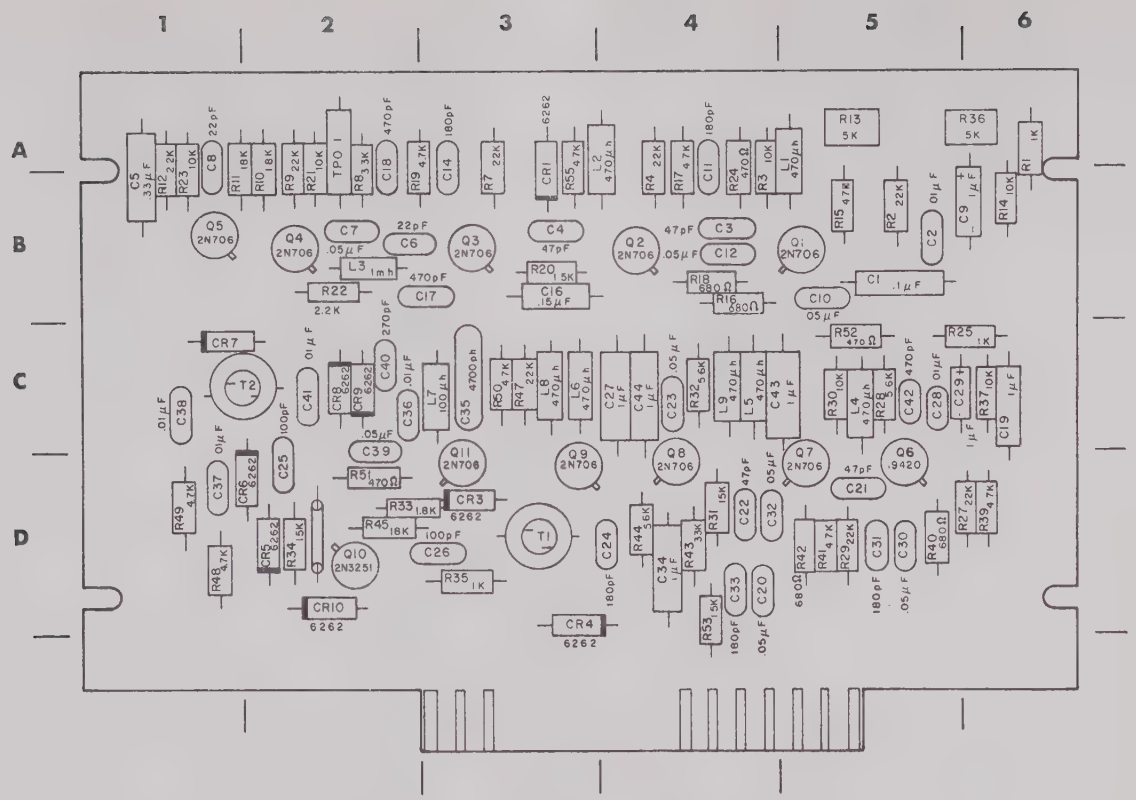
REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R11	A1	R0785
R12	A1	R0749
R13	A5	R2076
R14	B5	R0766
R15	B5	R0892
R16	B4	R1234
R17	A4	R0892
R18	B4	R1234
R19	A2	R0892
R20	B3	R0783
R21	B2	R0766
R22	B2	R1234
R23	A1	R0766
R24	B4	R1044
R25	C6	R0765
R26 N/A		
R27	D5	R0768
R28	C5	R0821
R29	D5	R0768
R30	C5	R0766
R31	D4	R0728
R32	C4	R0821
R33	D2	R1234
R34	D2	R1234
R35	D3	R0765
R36	A6	R2076
R37	C6	R0766
R38	N/A	R0766
R39	D6	R0892
R40	D5	R0821
R41	D5	R0892
R42	D5	R1234
R43	D4	R0780
R44	D4	R0821
R45	D2	R0821
R46	N/A	R0785
R47	C3	R0768
R48	D1	R0892
R49	D1	R0892
R50	C3	R0892
R51	D2	R1044

I. F. Amplifier, PC Board Assembly, Model 1253
(Sheet 2 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R52	C5	R1044
R53	D4	R0783
R54	N/A	R0783
R55	A3	R0892
T1	D3	17636
T2	C1	17636
Q1	B5	19420
Q2	B4	19420
Q3	B3	19420

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q4	B2	Q0130
Q5	B1	Q0130
Q6	D5	19420
Q7	D5	19420
Q8	C4	19420
Q9	D3	19420
Q10	D2	Q0174
Q11	D3	Q0130
TP1	A2	J0331

I. F. Amplifier, PC Board Assembly, Model 1253
(Sheet 3 of 3)



(Component layout diagram valid for Model 1254 only.
See Model 1255 Parts List for variations.)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	B5	C0236
C2	B5	C0233
C3	B4	C0533
C4	B3	C0533
C5	B1	C0239
C6	B2	C0378
C7	B2	C0672
C8	A1	C0378
C9	B6	C0524
C10	B5	C0672
C11	A4	C0707
C12	B4	C0672
C13	N/A	Not Used
C14	A3	C0707
C15	N/A	Not Used
C16	B3	C0524
C17	B2	C0542

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C18	A2	C0542
C19	C6	C0236
C20	D4	C0672
C21	D5	C0533
C22	D4	C0533
C23	C4	C0672
C24	D4	C0707
C25	C2	C0536
C26	D3	C0536
C27	C4	C0236
C28	C5	C0236
C29	C5	C0524
C30	D5	C0672
C31	D5	C0707
C32	D4	C0672
C33	D4	C0707
C34	D4	C0236

I. F. Amplifier, PC Board Assembly, Models 1254 and 1255
(Sheet 1 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C35	C3	C0633
C36	C2	C0233
C37	D1	C0233
C38	C1	C0233
C39	C2	C0672
C40	C2	C0539
C41	C2	C0233
C42	C5	C0542
C43	C5	C0236
C44	C4	C0236
CR1	A3	CR0150
CR2	N/A	Not Used
CR3	D3	CR0150
CR4	D3	CR0150
CR5	D2	CR0150
CR6	D1	CR0150
CR7	C1	CR0150
CR8	C2	CR0150
CR9	C2	CR0150
CR10	D2	CR0150
L1	A5	L0019
L2	A3	L0019
L3	B2	L0068
L4	C5	L0019
L5	C4	L0019
L6	C3	L0019
L7	C3	L0073
L8	C3	L0019
L9	C4	L0019
R1	A6	R0765
R2	B5	R0768
R3	A4	R0766
R4	A4	R0768
R5	N/A	Not Used
R6	N/A	Not Used
R7	A3	R0768
R8	A2	R0742
R9	A2	R0768
R10	A2	R0959
R11	A1	R0785

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R12	A1	R0749
R13	A5	R2076
R14	B5	R0766
R15	B5	R0892
R16	B4	R1234
R17	A4	R0892
R18	B4	R1234
R19	A2	R0892
R20	B3	R0783
R21	B2	R0766
R22	B2	R0749
R23	A1	R0766
R24	B4	R1044
R25	C6	R0765
R26 N/A		
R27	D5	R0768
R28	C5	R0821
R29	D5	R0768
R30	C5	R0766
R31	D4	R0728
R32	C4	R0821
R33	D2	R0959
R34	D2	R0728
R35	D3	R0765
R36	A6	R2076
R37	C6	R0766
R38	N/A	R0766
R39	D6	T0892
R40	D5	R1234
R41	D5	R0892
R42	D5	R1234
R43	D4	R0780
R44	D4	R0821
R45	D2	R0785
R46	N/A	R0785
R47	C3	R0768
R48	D1	R0892
R49	D1	R0892
R50	C3	R0892
R51	D2	R1044

I. F. Amplifier, PC Board Assembly, Models 1254 and 1255
(Sheet 2 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R52	C5	R1044
R53	D4	R0783
R54	N/A	R0783
R55	A3	R0892
T1	D3	17636
T2	C1	17636
Q1	B5	Q0130
Q2	B4	Q0130
Q3	B3	Q0130

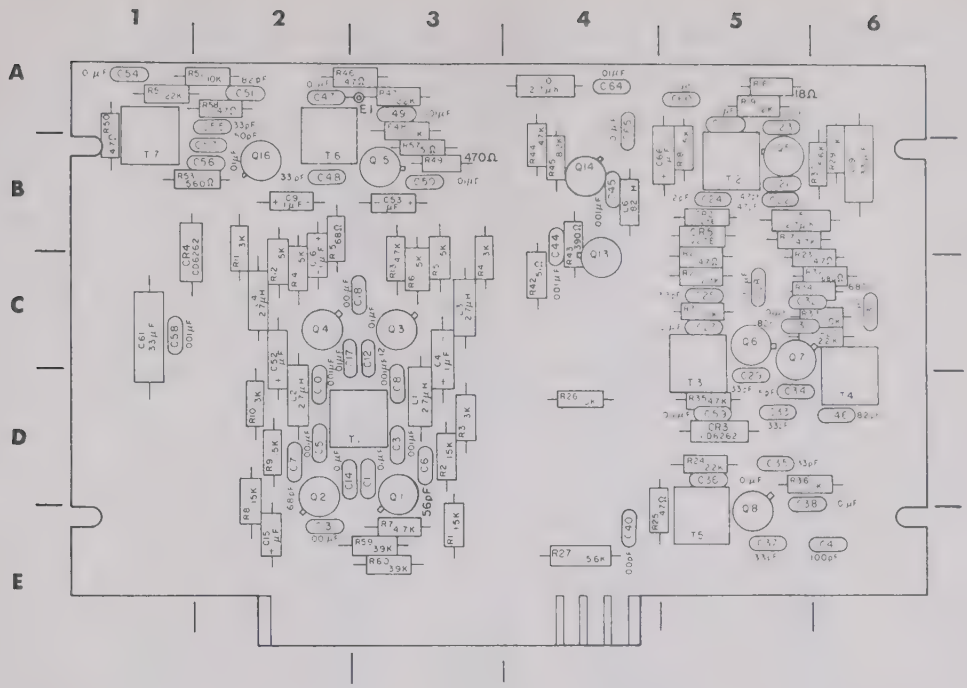
REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q4	B2	Q0130
Q5	B1	Q0130
Q6	D5	19420
Q7	D5	Q0130
Q8	C4	Q0130
Q9	D3	Q0130
Q10	D2	Q0174
Q11	D3	Q0130
TP1	A2	J0331

MODEL 1255 PARTS LIST (VARIATIONS ONLY)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C3	B4	C0378
C4	B3	C0535
C42	N/A	

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q1	B5	19420
Q6	C5	19420
R3	N/A	
R40	C5	R0821

I. F. Amplifier, PC Board Assembly, Models 1254 and 1255
(Sheet 3 of 3)



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	D3	C0562
C2	N/A	Not Used
C3	D3	C0424
C4	C3	C0524
C5	D2	C0424
C6	D3	C0534
C7	D2	C0635
C8	C3	C0424
C9	B2	C0524
C10	C2	C0424
C11	N/A	Not Used
C12	C3	C0562
C13	E3	C0424
C14	D3	C0562
C15	E2	C0524
C16	B2	C0524
C17	C3	C0562
C18	C3	C0424
C19	B6	C0239
C20	A5	C0562
C21	B5	C0533
C22	B5	C0533

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C23	A5	C0527
C24	B5	C0261
C25	C5	C0531
C26	N/A	Not Used
C27	C5	C0562
C28	C5	C0562
C29	C5	C0531
C30	C6	C0535
C31	C6	C0562
C32	C6	C0562
C33	D5	C0531
C34	D5	C0596
C35	D5	C0535
C36	D5	C0562
C37	D5	C0531
C38	D6	C0562
C39	D6	Not Used
C40	E5	C0536
C41	E6	C0536
C42	N/A	Not Used
C43	N/A	Not Used
C44	B4	C0424

Oscillator, PC Board Assembly, Model 1253
(Sheet 1 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C45	B4	C0424
C46	D6	C0539
C47	A2	C0562
C48	B2	C0531
C49	A3	C0424
C50	B3	C0562
C51	A2	C0535
C52	C2	C0524
C53	B3	C0524
C54	A1	C0562
C55	A2	C0531
C56	B2	C0562
C57	C2	C0539
C58	C1	C0424
C59	D5	C0424
C60	A5	C0562
C61	C1	C0701
C62	N/A	Not Used
C63	N/A	Not Used
C64	A4	C0562
C65	A4	C0562
C66	B5	C0524
CR1	N/A	Not Used
CR2	B5	CR0271
CR3	D5	CR0150
CR4	B2	CR0150
CR5	B5	CR0271
L1	D3	L0048
L2	D2	L0048
L3	C3	L0048
L4	C2	L0048
L5	B5	L0048
L6	B4	L0048
L7	N/A	Not Used
L8	N/A	Not Used
L9	N/A	Not Used
L10	A4	L0048
R1	E3	R2073
R2	D3	R2073
R3	D3	R2074

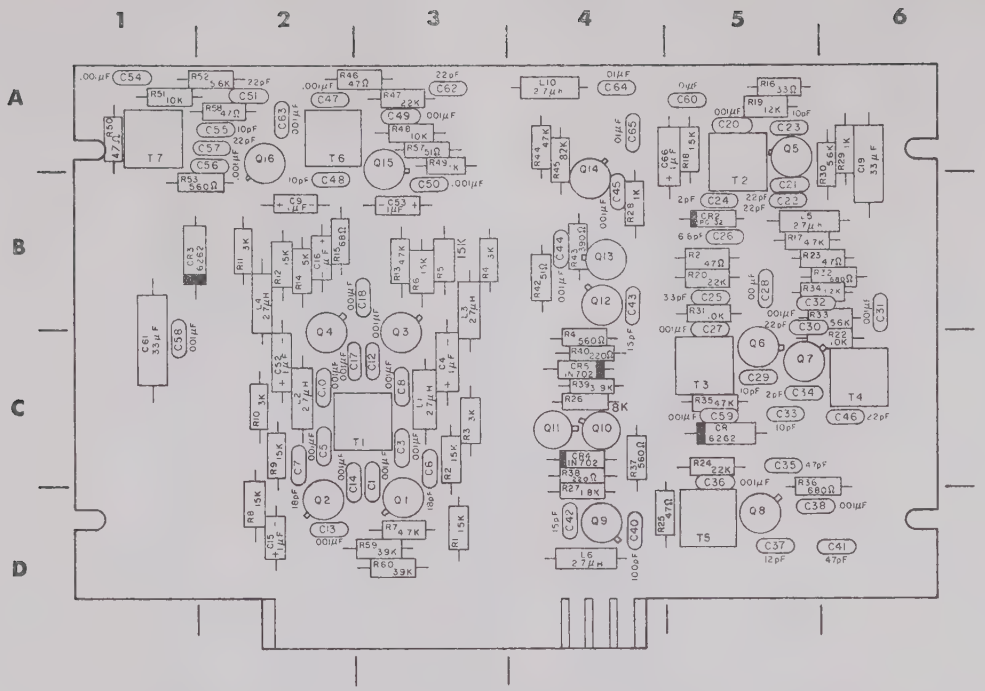
REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R4	B3	R2074
R5	B3	R2073
R6	C3	R2073
R7	E3	R0892
R8	E2	R2073
R9	D2	R2073
R10	D2	R2074
R11	B2	R2074
R12	B2	R2073
R13	B3	R0892
R14	C2	R2073
R15	B3	R1426
R16	A5	R1546
R17	B2	R0892
R18	B5	R0783
R19	A5	R0759
R20	C5	R0768
R21	B5	R0743
R22	C6	R0768
R23	B6	R0743
R24	D5	R0768
R25	E5	R0743
R26	D4	R0766
R27	E4	R0821
R28	N/A	Not Used
R29	A6	R0765
R30	B6	R0821
R31	C5	R0766
R32	C6	R1234
R33	C6	R0766
R34	C6	R1234
R35	D5	R0892
R36	D6	R0765
R37	N/A	Not Used
R38	N/A	Not Used
R39	N/A	Not Used
R40	N/A	Not Used
R41	N/A	Not Used
R42	C4	R1246
R43	B4	R0880

Oscillator, PC Board Assembly, Model 1253
(Sheet 2 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R44	B4	R0892
R45	B4	R0784
R46	A3	R0743
R47	A3	R0768
R48	A3	R0766
R49	B3	R1044
R50	A1	R0743
R51	A1	R0768
R52	A1	R0766
R53	B2	R0819
R54	N/A	Not Used
R55	N/A	Not Used
R56	N/A	Not Used
R57	A3	R1246
R58	A2	R0743
R59	E3	R0748
R60	E3	R0748
Q1	D3	19420
Q2	D2	19420
Q3	C3	19420

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q4	C2	19420
Q5	B5	19420
Q6	C5	19420
Q7	C5	19420
Q8	E5	19420
Q9	N/A	Not Used
Q10	N/A	Not Used
Q11	N/A	Not Used
Q12	N/A	Not Used
Q13	B4	19420
Q14	B4	Q0130
Q15	B3	Q0130
Q16	B2	Q0130
T1	D3	19191-1
T2	B5	19191-2
T3	C5	19191-3
T4	C6	19191-3
T5	E5	19191-3
T6	A2	19191-3
T7	A1	19191-3
E1	A3	E0203

Oscillator, PC Board Assembly, Model 1253
(Sheet 3 of 3)



REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C1	C3	C0424
C2	N/A	Not Used
C3	C3	C0424
C4	C3	C0524
C5	C2	C0424
C6	C3	C0697
C7	C2	C0697
C8	C3	C0424
C9	B2	C0524
C10	C2	C0424
C11	N/A	Not Used
C12	C3	C0424
C13	D2	C0424
C14	C2	C0424
C15	D2	C0524
C16	B2	C0524
C17	C2	C0424
C18	B3	C0424
C19	A6	C0239
C20	A5	C0424
C21	B5	C0378
C22	B5	C0378

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C23	A5	C0527
C24	B5	C0261
C25	B5	C0531
C26	B5	C0849
C27	B5	C0424
C28	B5	C0424
C29	C5	C0527
C30	B5	C0378
C31	B6	C0424
C32	B5	C0424
C33	C5	C0527
C34	C5	C0261
C35	C5	C0533
C36	C5	C0424
C37	D5	C0637
C38	D5	C0424
C39	N/A	Not Used
C40	D4	C0536
C41	D6	C0533
C42	D4	C0528
C43	B4	C0528
C44	B4	C0424

Oscillator, PC Board Assembly, Models 1254 and 1255
(Sheet 1 of 3)

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
C45	B4	C0424
C46	C6	C0378
C47	A2	C0424
C48	B2	C0527
C49	A3	C0424
C50	B3	C0424
C51	A2	C0378
C52	C2	C0524
C53	B3	C0524
C54	A1	C0424
C55	A2	C0527
C56	A2	C0424
C57	A2	C0378
C58	C1	C0424
C59	C5	C0424
C60	A5	C0562
C61	C1	C0239
C62	A3	C0378
C63	A2	C0424
C64	A4	C0562
C65	A4	C0562
C66	A5	C0524
CR1	C5	CR0150
CR2	B5	CR0244
CR3	B1	CR0150
CR4	C4	CR0126
CR5	C4	CR0126
L1	C3	L0048
L2	C2	L0048
L3	B3	L0048
L4	B2	L0048
L5	B5	L0048
L6	D4	L0048
L7	N/A	Not Used
L8	N/A	Not Used
L9	N/A	Not Used
L10	A4	L0048
L11	C4	H0654
L12	C4	H0654
R1	D3	R2073

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R2	C3	R2073
R3	C3	R2074
R4	B3	R2074
R5	B3	R2073
R6	B3	R2073
R7	D3	R0892
R8	D2	R2073
R9	C2	R2073
R10	C2	R2074
R11	B2	R2074
R12	B2	R2073
R13	B3	R0892
R14	B2	R2073
R15	B2	R1426
R16	A5	R1550
R17	B5	R0892
R18	A5	R0783
R19	A5	R0759
R20	B5	R0768
R21	B5	R0743
R22	C6	R0766
R23	B6	R0743
R24	C5	R0768
R25	D4	R0743
R26	C4	R0959
R27	D4	R0959
R28	B4	R0765
R29	A6	R0765
R30	A6	R0821
R31	B5	R0760
R32	B6	R1234
R33	B6	R0821
R34	B5	R0809
R35	C5	R0892
R36	C6	R1234
R37	C4	R0819
R38	C4	R0760
R39	C4	R0939
R40	C4	R0760
R41	C4	R0819

Oscillator, PC Board Assembly, Model 1254
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REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
R42	B4	R1246
R43	B4	R0880
R44	A4	R0892
R45	A4	R0784
R46	A3	R0743
R47	A3	R0768
R48	A3	R0766
R49	A3	R0765
R50	A1	R0743
R51	A1	R0766
R52	A2	R0821
R53	B2	R0819
R54	N/A	Not Used
R55	N/A	Not Used
R56	N/A	Not Used
R57	A3	R1246
R58	A2	R0743
R59	D3	R0748
R60	D3	R0748
Q1	D3	Q0177
Q2	D2	Q0177

REFERENCE DESIGNATOR	COMPONENT LOCATION	S-D PART NO.
Q3	C3	Q0177
Q4	C2	Q0177
Q5	A5	Q0177
Q6	C5	Q0177
Q7	C5	Q0177
Q8	D5	Q0177
Q9	D4	Q0177
Q10	C4	Q0177
Q11	C4	Q0177
Q12	B4	Q0177
Q13	B4	Q0177
Q14	B4	Q0130
Q15	A3	Q0130
Q16	A2	Q0130
T1	C2-3	19070-1
T2	A5	19070-2
T3	C5	19070-3
T4	C6	19070-4
T5	D5	19070-5
T6	A2	19070-6
T7	A1	19070-7

Oscillator, PC Board Assembly, Model 1254
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